NAVORD REPORT 4244

DELAY LINE TIME COMPRESSOR XT-IA

6 SEPTEMBER 1956

U. S. NAVAL ORDNANCE LABORATORY

WHITE OAK, MARYLAND

NAVORD Report 4244

DELAY LINE TIME COMPRESSOR XT-1A

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ABSTRACT: This report discusses briefly the relative advantages of several types of data processing systems but is mostly concerned with the development of the NOL Delay Line Time Compressor (DELTIC) XT-1A. The XT-1A is a sampling system which stores digital information in a number of DELTIC channels and then processes the data by the polarity coincidence correlation method.

The DELTIC samples the polarity of the signal under study at regular intervals and stores these samples in a circulating memory using a quartz delay line as the storage element. The ratio of the time between samples (T) to the time required to represent a sample (Δ) in the circulating memory is the number of times the data can be processed in a system using the time compressor while only one processing would be accomplished in a system without time compression. By suitable choice of parameters a Moving Time Series and a Stationary Time Series can be generated. The Stationary Time Series is delayed with respect to the Moving Time Series by(Δ) each circulation. Thus it is possible to generate a correlation function between the Moving Time Series and the Stationary Time Series. If the Moving Time Series and the Stationary Time Series are derived from the same signal an autocorrelation function is plotted. If they are derived from different signals, a cross-correlation function is plotted.

The DELTIC and control circuits are discussed both from a philosophic and a circuit-wise point of view. Block diagrams, schematics, component layouts, and photographs are given of the various portions of the system. Photographs are shown of typical waveforms including the output of the correlator for a number of different signal conditions.

U. S. NAVAL ORDNANCE LABORATORY
White Oak, Silver Spring, Maryland

NAVORD Report 4244 6 September 1956

This report describes the development of a specialized high-speed data processing system using polarity coincidence correlation methods. In its present state, the system is most effective in processing noise signals in a noise background in the lower part of the audio spectrum. However, it is expected that this type of system will have wide utility in processing data in many different fields. The work on this project was performed in the Physics Research Department and was supported by Foundational Research funds under Task FR-41. This report will be of interest to those working in the fields of: acoustics, correlation theory, electronics, data processing systems, and electronic computers.

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INTRODUCTION

History

The early work on the Delay Line Time Compressor (DELTIC) was done by V. C. Anderson. He completed the first workable DELTIC[1] in the spring of 1955 and checked the theoretical performance of this type of circuit at Harvard University. The Naval Ordnance Laboratory a few months later completed the development of a model usable under field conditions. The Navy Electronics Laboratory, San Diego, California, has also recently produced a DELTIC[2]. In the development of the first two DELTICS there was a free interchange of ideas which greatly expedited the work. The NOL equipment has been used in the field and has provided excellent and reliable performance.

Philosophy of Multiple Data Processing

It is an important problem to devise methods for multiple processing of data, particularly if it is necessary to provide continuous processing or to process large amounts of data. For small amounts of data the most efficient means usually is to record the data and play it back through suitable processing equipment as many times as is desired. This method, however, may require too much processing time if many processings are required or if the amount of data becomes quite large. In this case it is desirable to resort to more complicated methods. The number of operations, M, which can be performed while a simple playback system performs one operation can be thought of as the processing system gain or compression ratio.

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[1] V. C. Anderson, "The Deltic Correlator", Technical Memorandum No. 37, Acoustics Research Laboratory, Harvard University, 5 January 1956.

[2] T. G. Pine, Navy Electronics Laboratory Report 658, 9 February 1956.

Multiple processing systems can be used to speed up such operations as frequency spectrum analyses of a signal. These systems may also be used to plot very rapidly such functions as the cross-correlation between two signals versus time displacement.

There are three major methods in use today for producing multiple processings, each having advantages over the others in some respects. These will be discussed in turn.

1. Multiple Parallel Processing Systems. This utilizes one processing unit for each manipulation it is desired to perform. The processing units need handle only the bandwidth of the input signal. M in this case is merely equal to the number of processing units. This method is simplest if only a few operations are desired, but requires many processing units if many operations are desired. Dissimilarities between processing units may prove troublesome if outputs of several processing units are to be compared.

2. "True" Time Compression Systems. This consists of recording the signal at slow speed and playing it back at a higher rate into a single processing system, thus allowing many playbacks in a short time. In this case M is the ratio of playback to recording speed. Since frequencies played back are equal to those played in multiplied by the ratio of playback to recording speed the maximum M attainable with a given system is:

$$M_{max} = \frac{BW_p}{BW_i}$$

where BW_p is the bandwidth of the playback system and BW_i is the bandwidth of the input signal.

The capabilities of this system make it very attractive for many applications. The compressed signal retains its relative amplitude and phase characteristics and can be processed exactly like a signal of higher frequencies. Thus there is no loss in signal-to-noise ratio relative to a system processing the original signal. The limitation of this system lies in the reproducing system bandwidth, which presently cannot exceed a few hundred kilocycles, and for purposes of minimizing mechanical design and maintenance difficulties, should probably be only a few tens of kilocycles in a system in continuous use.

3. Sampling Systems. This method, as used in the Delay Line Time Compressor, samples nearly all of the non-redundant information and stores it in a circulating memory. In this case M is equal to the ratio of the time between samples to the time required to take one sample. In order to make this method practical it is necessary to reduce the data to binary form, positive or negative polarity.

Nearly all the non-redundant information is retained as long as three or more samples are taken per cycle of the highest frequency it is wished to process, with the chief loss being due to the reduction of the data to polarity information. Since the information is reduced to discrete bits the processing system bandwidth needs to be about 2.5 times the input bandwidth times the compression ratio, the factor of 2.5 being the price of the sampling system over a "true" time compression system. Large bandwidths are readily attainable in this system since it is all electronic. The system parameters are:

T = Time between samples

Δ = Time required to take one sample

$$\text{Compression ratio} = M = \frac{T}{\Delta} = \left(\frac{1}{2.5}\right)\left(\frac{BW_p}{BW_i}\right)$$

$$\text{Raw data represented by samples in line} = MT = \frac{T^2}{\Delta}$$

$$\text{BW of signal which is sampled effectively} = \left(\frac{1}{3}\frac{}{T}\right)$$

The minimum sample width which NOL has circulated satisfactorily in a memory is about 0.1 μs. By extending present techniques it should be possible to reduce this to about 0.04 μs, although this would require somewhat more complex equipment than is presently used. For less compression ability (broader sample widths requiring less bandwidth) the system becomes considerably less complex. The system described in this report has a bandwidth of 8.2 megacycles, which when divided by 2.5 to obtain an equivalent bandwidth for comparison with the "true" time compression system is still 3.3 megacycles.

The sampling method is by far the simplest and cheapest means yet devised for large compression ability, and it may prove competitive with, or for some applications, superior to

the other methods for low compression ability in regard to size, weight, initial cost, and upkeep.

Dielectric Integrator

In some instances more integration time may be required than one can obtain conveniently in a straight data processing system. This is true particularly where correlograms or other comparisons between two signals are to be plotted. Longer integration times may be obtained by any one of several means, one of which is the dielectric recorder developed by V. C. Anderson[1]. A working model with a numoer of modifications was built at NOL[3]. The NOL model is called a "dielectric integrator" but in this report both names are used interchangeably. This device averages a series of inputs point by point by successively superposing electric charges on a rotating dielectric drum synchronized with the processing system. The NOL version has an integration time variable from a small fraction of a second up to several hundred hours. The dynamic range is of the order of 55 db.

Report Plan

The above paragraphs presented a brief historical sketch of the development of a sampling data processing system using DELTICs, some remarks on the philosophy of three methods of multiple data processing, and a few words on an electrostatic device for increasing the integration time.

The next sections of this report will discuss the mechanism of operation of a moving time series circuit and a stationary time series circuit. Then the function and use of the control circuits, the polarity coincidence correlator, and the interconnecting cables will be discussed. The text material is supplemented by 40 illustrations, Figures 1 to 40 respectively.

Figures 1 to 5 are block diagrams of the various circuits. Photographs of the over-all system are presented in Figures 6 and 7. A schematic diagram and layout of the DELTIC chassis are shown in Figures 8 and 9 respectively. Photographs of the various chassis of the system comprise Figures 10, 13, 15, 18, and 21. The remaining Figures between 11 and 20 are schematic diagrams or layouts of other chassis in the system.

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[3] B. L. Snavely, "Dielectric Integrator and Delay Mechanism XD-1A", NAVORD 4243 (In preparation).

Photographs of the signals at various points in the system are presented in Figures 22 to 40. In order to simplify location of the points in the system where photographs were taken, each photograph has an identifying circled letter and the point in the system where the photograph was taken is identified by the same circled letter on the appropriate block diagram. These were taken using a Fairchild Model F-284 Polaroid Oscilloscope Camera and a Tektronix Model 545 Oscilloscope with a 53K/54K plug-in preamplifier and the appropriate low capacitance probe. Many of the DELTIC pictures were taken from the STS, since this allows simple synchronization of the sweep with the signal contained in the line. However, the wave shapes are equally applicable to the MTS.

After a short conclusion there is an Appendix which goes into considerable detail on the adjustment, calibration, and use of the various circuits. This section was added for the specialist interested in designing or using similar circuits and will be of less interest to most readers.

DELAY LINE TIME COMPRESSOR (DELTIC)

Operation of Moving Time Series

In the DELTIC the polarity of the signal under study is sampled at regular intervals, with the samples being inserted into a circulating memory. A pulse is inserted for one polarity, none for the other polarity. By proper system design the samples, which are separated in time, can be placed in the circulating memory in such a manner that there is no time separation at the output. By dropping out the oldest pulse when the newest is inserted, a high frequency high repetition rate representation of the sampled polarity information is obtained. At any given time it contains the previous N samples, where N is the number of samples the memory can store. This is accomplished by making the circulation time around the memory loop equal to one sample width (Δ) less than the time between samples (T). For this case the information in the line completes one circulation in (Δ) less than the time between samples, and thus all the information in the line appears to advance one (Δ) with each successive sample when viewed at intervals equal to the time between samples. Successive samples are then stored adjacent to one another. Since the (aN + b) position in the loop (where a is an integer) is the same as (b) position, it is evident that a sample must be removed from the loop after it has completed N circulations to avoid superposition of two pulses. Thus the oldest sample is removed and

replaced by a new sample so as to always retain the previous N samples within the memory.

The elements used in a Moving Time Series (MTS) are indicated in Figure 1. They consist of an input gate for inserting samples, a circulating loop (consisting of a vernier delay line, driver, reclocking gate, quartz delay line, amplifier, detector and recirculation gate), an output to a correlator or other comparison circuit, and an output to provide information for a Stationary Time Series (STS). The samples are circulated in the form of a pulse for one polarity of the input signal, no pulse for the other polarity of the input signal.

The heart of the circulating memory is the quartz delay line. Quartz was chosen as the delay medium for two reasons: delay stability and broad bandwidth. In order to obtain the best match to the quartz block, tuned transducers are used to convert the signal from electrical to acoustical at the input and back at the output of the quartz block. The pulses representing samples then must consist of a few cycles of the frequency to which the transducers are tuned. Since the delay line introduces a very high loss (nearly all of it being in the energy conversion process) a high gain bandpass amplifier is required. Then the signal is detected and smoothed slightly, still keeping the pulses as separate as possible. It is then passed through a normally open recirculation gate, a vernier coaxial delay line which is adjusted so as to make the time around the loop nearly the same for all channels used, and a driver amplifier. The pulses are repositioned with respect to one another and reinserted into the line by means of a saturable reclocking gate. This is essentially a saturable "and" circuit. The reclocking gate circuit corrects for errors in time around the loop. It also eliminates the effects of adjacent pulses partially merging due to insufficient bandwidth and non-linear phase shift in the loop, and thus allows closer pulse spacing with a given bandwidth. A sample may be dropped from the line by closing the recirculation gate for the duration of one pulse. A new sample may be inserted simultaneously by opening the input gate at the same time. The outputs of the recirculation gate and input gate are in parallel. An output amplifier to drive external circuits completes the Moving Time Series circuit.

Operation of Stationary Time Series

If the time around the loop is equal to the time between samples, the samples in the memory remain in the same position relative to successive sampling times rather than advancing as in the Moving Time Series. The circuit for the Stationary Time

Series (STS) is identical to the MTS circuit except for the time around the loop. The input for the STS consists of the output of a MTS. The input gate to the STS is opened for time T. During this time all the samples stored in the MTS appear at the input gate and are inserted in the STS. At the end of the period the input gate is closed. This time series then repeats itself in synchronism with the sampling pulse. Whenever it is desired to drop the old data and insert the most recent information the recirculation gate is closed for T and the input gate opened for the same period.

Control Circuits

Some means must be provided for furnishing the reclocking signals and the correct sampling and drop pulses to all channels. Provision must be made to synchronize all the signals so that the proper time phase and sequence is maintained. The three types of signals required are:

1. Reclocking Signal. In order to reposition the recirculation pulses a signal is required which effectively consists of a very narrow pulse with a repetition rate equal to $\frac{1}{\Delta}$ (separation equal to the interval between adjacent pulse centers in the line). Using this method the returned pulses need only occur at approximately the correct time to be reinserted in the line properly. In this way errors in time are not cumulative but are corrected with each circulation. This method will compensate for slight intra- and inter-channel variations in circulation time. This signal actually consists of a very large amplitude sinusoid with a frequency of $\frac{1}{\Delta}$. It is grid-current biased so that it never rises above 0 volts. The reclocking gate then operates Glass C with the grid overdriven negatively so much that as far as the tube current is concerned the sinusoid is effectively a very narrow-pulse with a repetition rate of $\frac{1}{\Delta}$.

2. Sampling Signal. Signals must be provided to enable the MTS to pick up new information and drop out old information simultaneously. The sampling pulses are approximately Δ in width, and have a repetition rate of $\frac{1}{T}$. The sampling input is of sufficient positive amplitude to open the input gate so that a new sample (consisting of either pulse or no pulse) may be inserted. The sampling drop pulse is of sufficient negative amplitude to close the recirculation gate so that one sample is dropped. By proper system design this is made to be the oldest

sample in the memory loop. The repetition rate of the sampling pulses is determined by the time around the loop of a DELTIC. The frequency of the reclocking oscillator is in turn controlled by the sampling input pulse. Thus, since all channels have identical electrical and physical characteristics, thermal and other environmental changes will cause the system to "breathe" as a unit so that no channel can get out of synchronism because its characteristics change in a different manner from other channels or from the sampling pulse and reclocking signals. This DELTIC loop is the master clock for the entire system.

3. Transfer Signal. Signals must be provided at fixed regular intervals to enable the STS to pick up new information and to drop out old information. The transfer pulses are approximately T in width, and occur simultaneously. The transfer input pulse is of sufficient positive amplitude to open the input gate so that a new time series of samples may be inserted. The transfer drop pulse is of sufficient negative amplitude to close the recirculation gate so that the old time series of samples is dropped. For some applications the interval between transfer pulses need not be regular, since the MTS and STS assume the same relative time displacements at the completion of each transfer pulse. Thus corresponding points on successive oscilloscope traces triggered by the transfer pulse will all lie the same distance from the start of the sweep, even though the sweeps may end at different points if the interval between transfer pulses is not regular. For some applications, such as when the DELTIC system is used in conjunction with the Dielectric Integrator, the inverval between transfer pulses must be regular. In this cited case a rotating drum must be synchronized with the transfer pulse repetition rate. An exact control can be obtained by counting sampling pulses. When the desired number has been reached the transfer pulse can then be triggered, simultaneously resetting the counter. This is the method used in the present system.

4. Control Circuit Functions. A block diagram of the Reclocking and Sampling Signal Chassis and Driver Chassis is given in Figure 2. The reclocking signal consists of the power amplified output of an oscillator with a frequency of $\frac{1}{\Delta}$. A comparison is made of the phase difference between the oscillator and the output of a DELTIC with a single pulse circulating in the loop. This phase difference is converted into a bias on a reactance tube which in turn controls the oscillator frequency so that the frequency is tied very closely to the DELTIC loop parameters. A separate buffer amplifier is used to provide the reclocking signal for each DELTIC in order to eliminate cross-coupling between channels. For convenience these are placed on

a separate chassis. Subsequent analysis of the reclocking signal driving problem showed that the cross-coupling effects noted early in the design were chiefly due to improper signal distribution. A more satisfactory solution would be to use a single power amplifier buffer stage with a separate cable for each reclocking gate. In this way the reclocking signal could not be other than precisely in phase at each reclocking gate. Also total buffer power requirements would be reduced.

The DELTIC with a single pulse circulating in the loop, which controls the reclocking oscillator and the sampling pulses, consists of a standard DELTIC with the circulation time equal to T and with additional circuitry in series with the loop to insure that only one pulse can circulate at a time. If the loop has more than one pulse in it the sampling pulse will occur oftener than T, thus the system must have a means of preventing circulation of more than one pulse. The passage of a pulse through a certain portion of the loop disables transmission through this portion for a period greater than $\frac{T}{2}$, but less than T. Thus the loop can sustain circulation of only one pulse. If another pulse enters the loop through some means such as a B+ transient it will be dropped out if it follows the other pulse by an amount less than the disabling time. If it is greater than the disabling time then the original pulse is dropped out and the new pulse now becomes the sampling pulse. As long as the likelihood of the injection of a new pulse is low this system is satisfactory. Since the disabling circuit is in series with the loop it is only necessary that after the passage of one pulse it be unable to pass another pulse for a period greater than $\frac{T}{2}$. The disabling circuit consists of a multivibrator which is triggered by the circulating pulse, thus transferring the pulse to its output. As long as the circuit remains "flipped", and for a short time after it returns to its original state, it is impossible to cause another pulse to appear at the output. Thus by making this disabled time greater than $\frac{T}{2}$ only one pulse is circulated. The series circuit used in addition to the DELTIC consists of an amplifier (to drive the disabling multivibrator with sufficient amplitude to reduce uncertainties regarding the time of the leading edge of the pulse), the disabling multivibrator, a pulse shaper, and a power amplifier to provide the sampling pulses to the MTS. The output of the multivibrator consists of a rectangular wave of current with the positive and negative portions each being of the order of $\frac{T}{2}$ in duration. A piece of shorted coaxial delay line is used to transform this into a voltage pulse of approximately Δ duration. A diode with appropriate polarity is used to short out

the negative voltage pulse. A single tube phase splitter power amplifier is used to provide sampling pulses of both polarities to the MTS. Suitable attenuation is introduced in the pulse fed to the master loop since it is reinserted at the input to the driver.

Since the oscillator frequency has a period of Δ and the sampling pulse occurs at intervals of T. then $\frac{T}{\Delta}$ cycles of the oscillator occur between sampling pulses. Since many cycles of the sinusoid thus occur between phase comparisons with the sampling pulse it is theoretically possible for the oscillator to lock in on any frequency for which an integral number of cycles takes T time. In a practical system the number of possible modes is greatly reduced, but several will exist, the number depending on the total frequency swing it is possible to obtain when the phase difference varies from 0 to 180°. The phase relationship between the sampling pulse and the oscillator will be somewhat different on different modes, therefore it is desirable to operate on a given mode at all times. To accomplish this it is merely necessary to return the grid of the reactance tube to some desired dc voltage. When the circuit is returned to its normal condition the long time constant of the circuit gives the oscillator a tendency to lock in on the mode which will return approximately the same voltage to the grid of the reactance tube as the dc voltage which was applied. The circuit which sets the oscillator on the desired mode is referred to as the mode selector.

In case the sampling pulse is dropped out of the master loop by some means such as a transient, it is necessary to reinsert a pulse into the loop. This can be done automatically by having the disabling multivibrator generate a pulse if an interval greater than T goes by without a pulse entering the multivibrator. By setting the constants of the circuit such that the multivibrator will free run at a rate somewhat slower than $\frac{1}{T}$ the automatic insertion feature can be incorporated without interfering with the other functions of the disabling circuit.

In order to simplify setting the timing throughout the system a voltage with a repetition rate of the reclocking signal is derived which is suitable for use as a trace brightener on an oscilloscope. This is obtained from the screen of the power amplifier used to drive the reclocking signal buffer amplifiers by using a small unbypassed screen dropping resistor, and is phased properly with respect to the reclocking signal by using an appropriate length of coaxial delay line cable between the chassis and the oscilloscope.

A block diagram of the Transfer Signal Chassis is given in Figure 3. It is necessary to provide the proper interval between transfer pulses. Furthermore, it is desirable that the transfer pulse be almost exactly T in duration, since a slight change in length can cause a large error in the number of samples transferred. If either less or more than exactly one line full of samples are transferred, errors in correlation will occur. These errors increase as the difference between the number of pulses transferred and the number of pulses contained in the loop increases. The circuit used to furnish the desired pulse duration and repetition rate obtains approximately the correct time for pulse initiation by counting sampling pulses. However, since the counter has a relatively slow rise time, and since there is some delay between an input pulse and the count appearing at the output, this counter is merely used to "enable" another portion of the circuit. The latter circuit generates a pulse which is triggered on by the first sampling pulse after it has been enabled and triggered off by the second sampling pulse. The enabler is a single-shot multivibrator driven by the counter which remains in its unstable state for at least 2T, but less than 3T after it has been triggered. Its output is a pulse with approximately the desired interval and a duration between 2T and 3T. If this signal is fed to one input of an "and" circuit, and the sampling pulse to the other, the output of the "and" circuit consists of two sharp pulses separated by exactly T with exactly the desired interval between pulse pairs. This signal is used to trigger a multivibrator from one state to the other and back again, so that the output is a pulse of T duration at the desired repetition rate. By using the method described the transfer pulse duration and repetition period are controlled within a very small fraction of the time interval Δ.

The transfer signal circuit consists of a pulse shaper which amplifies and stretches the transfer pulses so that they are suitable for the counter, a counter (pre-set for the desired number of sampling pulses it is desired to have between transfer pulses), the enabler, an "and" circuit, the multivibrator circuit, and a power amplifier. The pulse counter has an output suitable for synchronizing the dielectric recorder motor drive circuit. A single tube phase-splitter power amplifier is used to provide transfer signal pulses of both polarities to the STS. An output is provided through a decoupling tube to provide positive synchronizing pulses coincident in time with the transfer pulses. The output of the multivibrator must be a positive pulse to provide the proper drive for the power amplifier. To insure the proper output the circuit is given a preference for one state such that it will not remain in the other state for a period as long as the interval between transfer pulses. In this way the

circuit automatically assumes the correct state such that a positive pulse is fed to the power amplifier.

CORRELATOR

In many cases it is desired to produce either the autocorrelation function of a signal under observation or the cross-correlation function of two signals. The DELTIC is ideally suited to the generation of such functions on a polarity coincidence basis. The relationship between polarity-coincidence correlation and multiplier correlation is well known, and is (for signals with a Gaussian distribution of amplitudes):

$$R = \% \text{ Polarity Agreements} - \% \text{ Polarity Disagreements}$$

$$= \frac{2}{\pi} \arcsin \rho$$

where R = polarity-coincidence correlator meter reading

ρ = multiplier correlator meter reading

Polarity-coincidence correlation can be measured by comparing the output of an MTS DELTIC with that of an STS DELTIC. Generation of the correlation function results from the relative displacement in discrete steps between the MTS and the STS, which is the result of the difference in time, Δ, around the loop between the two. During the period T after loading the STS from the appropriate MTS, the two loops contain polarity information regarding their respective input signals with a given time displacement (which will depend on the time required to transfer the information from the MTS to the STS). Since the two series progress around their respective loops at the same rate the relative time displacement remains the same during the period T. Since the output of each line is an ordered succession of pulses (or lack of pulses) representing the succession of polarities in a corresponding portion of the original data, a pulse-by-pulse comparison between the outputs of the two series for a period T will be a measure of the polarity-coincidence correlation for the particular time displacement which exists. During the next period T the MTS will have advanced an additional Δ with respect to the STS, so a comparison of the outputs of the lines for T will be measure of the polarity-coincidence correlation for this new time displacement.

Through the use of the DELTIC, $\frac{T}{\Delta}$ comparisons are made in a period T (the interval between samples in the raw data). Each

T the MTS advances one sample with respect to the STS. Thus in each time interval T a point on the correlogram is generated which is based on $\frac{T}{\Delta}$ samples (or $\frac{T^2}{\Delta}$ time in the raw data), and which represents a time displacement between the two series of raw data of T greater than the previous point.

In the correlator used in conjunction with the NOL DELTIC, the correlation is measured by taking the negative of the per cent disagreements in polarity over the period T, rather than measuring the per cent agreements in polarity minus the per cent disagreements in polarity. This can be done with no loss in information since the sum of the per cent disagreements and the per cent disagreements is 100%. The expression for the disagreements in polarity in terms of correlation is $-(\%\ \text{Disagreements}) = \frac{R}{2} - \frac{1}{2}$. Removal of the dc term and reproportioning the scale factor gives:

$$-(\%\ \text{Disagreements}) \propto R$$

In a low frequency correlator the correlation can be obtained from the clipped signals by addition, full-wave rectification and averaging. However, at the repetition rates used in the DELTIC it is very difficult to keep adjacent pulses in the train independent, thus necessitating another approach. The one used is to count the number of disagreements in polarity that occur during one circulation time. This is accomplished by adding the signals from the two channels together so that if both signals are positive a +1 (for example) results, if the signals are opposite in phase a 0 results, and if both signals are negative a -1 results. The composite signal is then impressed upon a saturable decision gate biased so that an output is possible only when both signals are positive. By introducing the reclocking signal into another grid of the decision gate the decision as to the polarities is made each Δ, and the decision time is confined to a small fraction of a Δ which is positioned in the center of the composite pulse for maximum reliability. Thus each time both signals are positive a short pulse of current of the same amplitude and phase is emitted by the decision gate. The composite signal is also impressed upon a second decision gate identical to the first except that it is biased to produce a pulse whenever either both signals are positive or are opposite in phase. Extracting the difference between the outputs of the two decision gates and integrating over approximately T results in the per cent differences in polarity, which is analogous to the correlation. If the outputs of the decision gates have different amplitudes the result is merely a scale factor change in the dynamic

correlation. In order to reduce the high frequency response requirements in the difference amplifier some integration can be included in the outputs of the decision gates. As long as this is short compared to the total integration time there will be no effect on the correlation even if there is a considerable difference in integration times between one decision gate output and the other.

The block diagram of the correlator is shown in Figure 4. The signals from the two DELTIC channels are first amplified and clipped individually to insure that they are of approximately the same amplitude and rise time, thus simplifying the operation of the decision gates. The clipped signals are added by tying the plates of the clipper amplifiers together. The decision gates are saturable "and" circuits similar to those used in the circulating loops except that they operate at a much lower level. The difference amplifier, simple RC integrator and an output amplifier complete the correlator.

Interconnecting Cables

A large number of interconnecting cables must be utilized to distribute and transfer signals. In order to facilitate proper time phasing and synchronization, and to reduce capacitive loading effects, all cables conveying pulse information are high impedance delay type coaxial cables. The reclocking signal cables are standard 100-ohm coaxial cables since in this case the capacitance could easily be tuned out. A block diagram of the interconnecting cables between chassis in the system is shown in Figure 5. Cables internal to the chassis are shown in Figures 1 and 2.

The total time around the loop in the reclocking and sampling signal generator shown in Figure 2 must be T. This, in combination with the length of the quartz delay line and the transit time through the loop circuitry fixes the total length of the vernier coaxial delay line. Since a certain phase will be maintained between the reclocking signal and the sampling pulse at the phase comparator, and since the reclocking signal and the sampling pulse must enter the reclocking gate simultaneously to maintain proper circulation, the portion of the vernier coaxial delay line lying between the power amplifier and the driver is fixed. This in turn fixes the length of the vernier coaxial delay line between the detector and amplifier.

The time around the loop in the MTS is $(T - \Delta)$ as shown in Figure 1. This, in combination with the length of the quartz delay line and the transit time through the loop circuitry fixes

the length of the vernier coaxial delay line. The sampling drop and input pulses must have the proper timing so that the dropped or inserted signal pulse or no-pulse will arrive at the reclocking gate at the correct time with respect to the reclocking signal. Thus sampling drop and input pulses must arrive at the recirculation and input gates respectively at a time earlier than the positive peak of the reclocking signal by an amount equal to the transit time through the gates, vernier coaxial delay line, and driver. This in combination with the relative phase between the reclocking signal and the sampling signal at the point of origin fixes the length of the coaxial delay lines which furnish the sampling signal to the MTS.

The time around the loop in the STS is T as shown in Figure 1. This, in combination with the length of the quartz delay line and the transit time through the loop circuitry fixes the length of the vernier coaxial delay line. The length of the coaxial delay cable which connects the output of the MTS to the input of the STS must be such that the input pulses arrive at the reclocking gate at the proper time to be inserted. The same principles apply here as in the sampling signal for the MTS.

The relative phase between the transfer signal and the reclocking signal normally is not critical since the transfer signal has a duration of T. If the phase is incorrect one sample may fail to be transferred, but normally this is such a small part of the information contained in the loop that its loss may be disregarded. If, however, it is necessary to assure transfer of the exact number of samples, the same principles apply here also as in the sampling signals of the MTS. Note, however, that there is an additional length of coaxial delay line to be taken into account in this case, namely the line connecting the reclocking and sampling signal chassis to the transfer signal chassis (this cable may be merely chosen to be a convenient length to connect the two chassis since no synchronizing problems exist here).

Since the samples inserted into the STS experience a considerable delay in passing from the output of the MTS to the reclocking gate of the STS, the STS is displaced several digits behind the MTS on the first circulation after transferring the samples. In order to be able to start the correlation sweep with no delay when using a correlator and to eliminate "nonsense" comparisons where the signals do not overlay correctly in time it is necessary to delay the output of the MTS sufficiently before it reaches the correlator so that it is once again in phase with the STS on the first circulation. This is accomplished

by making the coaxial delay line from the MTS to the correlator longer than for that of the STS by an appropriate amount. Since the signals are again reclocked in the correlator the lengths of the coaxial delay lines leading to the correlator must be such that the input pulses arrive at the correlator at the proper time.

CONCLUSION

Research and development work on a specialized high-speed data processing system has been described, including an exposition of the design philosophy, the basic principles of operation, and the adjustment and calibration of the complete system.

A discussion of the circuit details and the quantitative aspects of circuit design are given in Appendix I.

ACKNOWLEDGMENT

The work reported here was performed in the Acoustics Division. T. F. Johnston reviewed and edited the report.

APPENDIX I

DELTIC AND AUXILIARY CIRCUIT DETAILS

Moving Time Series Circuits

The schematic diagram, component layout, and a photograph of the DELTIC circulating loop are shown in Figures 8, 9, and 10, respectively. They are equally applicable to the MTS and STS.

In order to adequately process signals with a bandwidth of 6700 cps it is necessary to sample every 50 microseconds. Using a sample width of 0.1 microsecond gives a system capacity of 500 digits, or the equivalent of 25 milliseconds of raw data.

The quartz delay lines used are nominally 50 microseconds in length and have a carrier frequency of 40 megacycles. The attenuation at the center frequency depends upon the particular line chosen, and varies between 34 and 44 db into a 100 ohm resistor when the transducer capacitance is tuned out, with an average of 40 db. The attenuation at 40 $\pm$5 megacycles relative to that at 40 megacycles varies from 0 to -4 db, with an average of -1.8 db. The spurious response varies from 35 to 42 db below the main signal, with an average of 37 db. The delay time varies by $\pm$0.005 microseconds from the average delay of 49.975 microseconds. The listed characteristics exceed the design specifications in every case. Since the velocity of propagation of the acoustic wave in fuzed quartz varies with temperature all the delay lines are mounted within an insulated box. The box is not temperature controlled since the control circuits have been designed so that temperature variations cause the timing of the control signals to vary in the same manner as the DELTIC loops. Thus temperature effects are nullified. As long as the temperature difference between lines does not vary more than 3°C the differences in apparent lengths vary less than 0.01 microsecond.

The reclocking gate output coupling circuit, the quartz delay line output coupling circuit, and the band pass amplifier are in cascade. For optimum transient response, simplicity in construction, and freedom from critical adjustments all stages are designed for the same bandwidth. The quartz delay line itself has a much broader response than any stage, so its effect is neglected. In addition to bandwidth the sharpness of the cutoff must be considered in optimizing the transient response of a

system, since a sharp cutoff causes non-linear phase shift near the edge of the pass band, resulting in excessive ringing. The circuit chosen for the amplifier was the band pass equivalent of a low pass shunt-peaked circuit with k = 0.63. Since the input impedance of the quartz delay line consists almost entirely of a large capacitive reactance, the mismatch on the coaxial cable connecting the quartz delay line to the chassis could cause large undesirable reflections, resulting in poor transient response. This trouble is circumvented in two different ways. The cable from the reclocking gate to the quartz delay line is made as short as possible (about 2 inches) to reduce the seriousness of the mismatch. In the case of the output of the quartz delay line the coil used in tuning out the quartz delay line capacitance is mounted directly at the output of the delay line, and the end of the coaxial cable connected to the output to the band pass amplifier is resistively terminated, thus greatly reducing the mismatch. The length of this coaxial cable is not critical, so the distance between the output of the quartz delay line and the input to the amplifier can be dictated by convenience. For ease of construction with relatively small sacrifice in performance no shunt peaking is employed in this one stage. The reasons for the two different approaches to the termination problem were to obtain maximum performance and flexibility of parts placement with relatively simple construction methods. Each individual stage exhibits a bandwidth of about 15 megacycles between the 3 db points centered around 40 megacycles, while the bandwidth for 6 cascaded stages is about 8 megacycles.

The amplifier consists of 4 cascaded stages, and has a maximum gain of 70 db. The gain of the first three stages can be varied by manually controlling the grid bias. Since the input to the fourth stage is of relatively large amplitude the grid bias is fixed by use of a bypassed cathode resistor. This is done in order to eliminate any partial detection of the signal in this stage since detection in this stage will tend to cancel the action of the detector which immediately follows.

The output of the last stage of the amplifier is used to drive a plate detector using grid leak bias. For optimum detector performance the signal level is adjusted by varying the gain of the amplifier so that the grid bias as measured on the grid side of the grid leak is approximately -6 volts. A Type 5725 pentode with high transconductance on both control and suppressor grids is used. By driving the suppressor of the detector sufficiently negative (about -10 volts) the detector is prevented from passing any plate current. In this way the detector is used as a gate for dropping samples. The suppressor is normally operated at +5 volts (which causes the suppressor transconductance to drop

essentially to zero) to eliminate undesirable effects from extraneous low level signals on the suppressor. There was a slight tendency of the circuit to motorboat (which would continue until stopped) while the memory was being initially loaded (caused by high initial gain). Hence a pre-bias of 2.7^{V} was put on the detector control grid to limit the initial gain. The detected pulses are about 6 volts peak-to-peak.

The bandpass portion of the circulating loop is adjusted for proper operation by using standard sweep generator techniques. A 270 ohm resistor is provided in the DELTIC which can be used as the plate load of the detector for these adjustments. The grid resistor in the detector is changed to 100 k for these measurements and the detector used as a linear amplifier.

The output of the detector-drop gate is in parallel with the output of the input gate. The input gate (which is a 5725) is normally cut off by biasing the suppressor to -10 volts. To insert a sample, the suppressor is driven to +5 volts (thus saturating the suppressor), simultaneously driving the suppressor on the detector-drop gate to -10 volts. The sense of the sample (i.e., positive or negative) is determined by the voltage on the control grid and will result in plate current flowing (positive sample = pulse inserted into the loop or no plate current flowing; negative sample = no pulse inserted into the loop). For optimum pulse insertion the gain of the input gate is controlled by varying the screen grid potential until the inserted pulse is of slightly greater amplitude at the driver plate than the recirculated pulse. The control grid bias is grid current derived. Photographs of the sampling input and drop pulses are given in Figures 22 and 23 respectively. The small secondary pulse shortly after the sampling pulse is caused by improper termination of the coaxial delay line, but is sufficiently small that the grid remains saturated or cut off as the case may be.

The 2200 ohm vernier coaxial delay line is driven by the combined outputs of the detector-drop gate and the input gate. This line is trimmed to provide the proper time around the loop. In order to minimize reflections at the output end of the line due to the mismatch caused by the input capacitance of the following stage, a constant-k terminating half section is utilized. It was found desirable to terminate the driven end of the line in its characteristic resistance, although it was not necessary to use a terminating half section in this case. The low pass characteristic of the coaxial delay line is utilized to filter out the carrier frequency components and

smooth the pulses. The smoothed pulses are about 4 volts peak to peak.

The driver stage, whose input is the vernier coaxial delay line, must generate a positive 30-volt pulse with 0.04 microsecond rise time to properly actuate the reclocking gate. A two-terminal linear phase shift plate-coupling network is used with a tapped plate resistor which provides for a lower level signal to the output tube.

The signal returned around the loop is introduced into the reclocking gate (a 5725 tube) on the suppressor. The negative swings (negative sample) of this signal are clamped to -10 volts with a germanium diode, while the positive peaks (positive sample) range upward to +20 volts. The reclocking signal is fed into the control grid, and consists of a 10 megacycle sinusoid with an amplitude of 100 volts peak-to-peak. Using grid current bias to clamp the positive swing to 0 volts, the signal is sufficiently negative to cut the tube off during the entire cycle except for a period of time equal to about one-half cycle of forty megacycles, which occurs at the time of the positive peak of the reclocking signal. With the operating conditions outlined it is necessary for both control and suppressor grids to be positive for the plate to pass any current. If the suppressor grid is sufficiently positive at the proper time the tube generates a plate current pulse consisting of a half cycle of forty megacycles, thus generating a voltage pulse in the plate tank, the effect of which reappears at the suppressor grid of the reclocking gate one circulation later. As long as the recirculated (or new information) signal has driven the suppressor more than 5 volts positive at the time of the peak of the reclocking signal, all pulses created by the reclocking gate are identical and are about 2.5 volts peak-to-peak in amplitude. This allows a shift between the peak of the reclocking signal and the recirculated signal up to about ± 0.02 microseconds depending upon the exact shape of the returned pulse. The timing of the sampling drop pulse is fairly critical and should be within 0.01 microseconds of the optimum value to insure proper operation. Generation of a somewhat larger or squarer sampling drop pulse in order to cut the detector-drop gate off for a larger portion of the 0.1 microsecond sample width would reduce the timing accuracy requirements. A 10 ohm cathode resistor is used to provide a convenient low impedance observation point at the reclocking gate for setting up and troubleshooting.

The output stage is used to provide signals for driving the transfer input gate of an STS at a level of 3 volts peak-to-peak through a 950 ohm delay line coaxial cable (a photograph

of this is shown in Figure 24) and for driving the correlator at a level of 20 volts peak-to-peak through a 2,200 ohm delay line coaxial cable. A terminating half section is used to minimize reflections on the 2200 ohm line. The lower impedance cable is used to drive the input gate to retain the best possible pulse shape for insertion into the STS. The higher impedance cable is used to drive the correlator to provide the largest possible voltage commensurate with reasonable pulse shapes. The negative swings of the signal on the control grid are clamped to -4.4 volts which nearly cuts the output tube off, giving the maximum current swing available on a positive pulse. Isolation between cathode and plate load is obtained by using a 5725 with the suppressor bypassed to ground. A sufficiently high dc potential is applied to the suppressor so that the suppressor transconductance is zero even at the peak cathode voltage, thus the suppressor does not tend to reduce plate current on the pulse peaks.

In setting the timing of an MTS it is desirable to trigger the oscilloscope from the output tube of the master DELTIC (the one with a single pulse circulating in the loop). This synchronizes the sweep with the sampling rate. In the initial setup it is merely necessary to turn the gain of the amplifier down sufficiently to prevent stable recirculation to be sure that the circulation time of the MTS is one digit less than the time between sampling pulses. The first circulated pulse should be one digit earlier than the sampling pulse.

Since there is some dispersion in the circulating system the interval between recirculated pulse peaks in a pulse train at the input to the reclocking gate is not quite uniform. For optimum performance the time around the loop is set such that the first and last pulses in a train are at the same amplitude at their respective instants of reinsertion (at the time of the peak of the reclocking signal). This is done very simply by using the oscilloscope trace brightening (which is done at the repetition rate of, and in phase with, the 10 megacycle reclocking signal) in conjunction with the fact that the trace on the oscilloscope contains pulse trains displayed at all possible integral delays of 0.1 microsecond (since the circulation time is not synchronized with the interval between triggers). The first and last pulses in a train are thus superimposed, and the vernier coaxial delay line cable is merely varied in length until the brightened spot on the trace is superimposed on the time at which the first and last pulses have the same amplitude

The sampling input and drop pulses are readily adjusted to the proper time since they have the same repetition rate as the

oscilloscope trigger, and thus they appear stationary on the oscilloscope screen.

A photograph of the signal at the input to the reclocking gate is shown in Figure 25. It is seen that the time around the loop is about right, that the sampling input pulse is slightly early, and that the time of the sampling drop pulse is upwards of 1/10 digit early. Two sets of input and drop pulses are observed. This results from the last circulated sample before the sampling pulse being either pulse or no pulse, and shows the crosstalk between adjacent samples due to the restricted bandwidth of the system. The amount shown is not serious. The oscilloscope probe was not connected directly into the circuit as the added capacitance disturbs the pulse shape, and thus the effective time around the loop. For timing measurements the probe should be merely placed sufficiently close to the reclocking gate input to electrostatically couple an adequate amount of signal to the oscilloscope.

It has been found that one DELTIC chassis can be replaced by another with no necessity for readjusting the timing of any of the coaxial delay lines. There is apparently very little dispersion in the transit times through different DELTIC chassis.

For these adjustments and for others in various portions of the system and for troubleshooting it is desirable to use a signal between 200 cps and 5000 cps as the signal to be sampled by the DELTIC. In some cases it is desirable to have the signal synchronized with the sampling interval, in others it is best to have it unsynchronized. A convenient source of several sychronized frequencies is the output of the various counters in the transfer signal chassis. A high impedance pick-off must be used to prevent malfunctioning of the counters, however.

Stationary Time Series Circuits

The circuits used in the STS are identical with those used in the MTS except for three details. The transfer input gate is provided with a 1,000 ohm resistor to properly terminate the coaxial delay line from the MTS, and a decoupling capacitor to allow it to develop grid current bias. The 2200 ohm vernier coaxial delay cable is trimmed to make the STS 0.1 microsecond further around the loop than the MTS. Since the output tube of the STS does not drive another memory loop the cathode is loaded with a 1000 ohm resistor to make the output level to the correlator the same as for an MTS.

Since the circulation time of the STS is the same as the interval between sampling pulses, if the signal being sampled

A block diagram of the Transfer Signal Chassis is given in Figure 3. It is necessary to provide the proper interval between transfer pulses. Furthermore, it is desirable that the transfer pulse be almost exactly T in duration, since a slight change in length can cause a large error in the number of samples transferred. If either less or more than exactly one line full of samples are transferred, errors in correlation will occur. These errors increase as the difference between the number of pulses transferred and the number of pulses contained in the loop increases. The circuit used to furnish the desired pulse duration and repetition rate obtains approximately the correct time for pulse initiation by counting sampling pulses. However, since the counter has a relatively slow rise time, and since there is some delay between an input pulse and the count appearing at the output, this counter is merely used to "enable" another portion of the circuit. The latter circuit generates a pulse which is triggered on by the first sampling pulse after it has been enabled and triggered off by the second sampling pulse. The enabler is a single-shot multivibrator driven by the counter which remains in its unstable state for at least 2T, but less than 3T after it has been triggered. Its output is a pulse with approximately the desired interval and a duration between 2T and 3T. If this signal is fed to one input of an "and" circuit, and the sampling pulse to the other, the output of the "and" circuit consists of two sharp pulses separated by exactly T with exactly the desired interval between pulse pairs. This signal is used to trigger a multivibrator from one state to the other and back again, so that the output is a pulse of T duration at the desired repetition rate. By using the method described the transfer pulse duration and repetition period are controlled within a very small fraction of the time interval Δ.

The transfer signal circuit consists of a pulse shaper which amplifies and stretches the transfer pulses so that they are suitable for the counter, a counter (pre-set for the desired number of sampling pulses it is desired to have between transfer pulses), the enabler, an "and" circuit, the multivibrator circuit, and a power amplifier. The pulse counter has an output suitable for synchronizing the dielectric recorder motor drive circuit. A single tube phase-splitter power amplifier is used to provide transfer signal pulses of both polarities to the STS. An output is provided through a decoupling tube to provide positive synchronizing pulses coincident in time with the transfer pulses. The output of the multivibrator must be a positive pulse to provide the proper drive for the power amplifier. To insure the proper output the circuit is given a preference for one state such that it will not remain in the other state for a period as long as the interval between transfer pulses. In this way the

loads for fast rise times. These were chosen to be 5725's for isolation between plate and cathode. The suppressors are run sufficiently positive with respect to the cathodes so that suppressor transconductance is zero. A non-critical adjustment is provided to set the free-running rate high enough so that it can be triggered every 50 microseconds, but low enough so that it cannot be triggered as often as every 25 microseconds. The shaped pulse out of the multivibrator is 20 volts peak-to-peak. The power amplifier output stage is a sharp cutoff high transconductance pentode phase splitter kept normally at cutoff by a 5.6 k cathode resistor. The pulse current exceeds 50 ma with an average of less than 1 ma. Outputs are taken from the plate and cathode of this tube at 15 volts peak-to-peak to provide the positive and negative sampling input and drop pulses, the input to the master DELTIC (through a voltage divider), and the phase comparator. The input to the phase comparator is decoupled to prevent variations in the 26 volts from feeding back to the common sampling signal output through the voltage dividers in the input gates of the MTS and the coaxial delay line cables, thus resulting in apparent changes in phase between the sampling pulse and the reclocking pulse.

The phase comparator is a Type 5725 operating as a dual control amplifier. The parameters of the feedback loop are set such that the normal equilibrium point is for the peaks of the reclocking signal and the sampling signal to be considerably out of phase at the phase comparator. Since the reclocking signal is effectively a very narrow pulse the plate current will consist of a very narrow pulse whose amplitude will depend upon the amplitude of the sampling signal at the time of the peak of the reclocking signal. The peak amplitude of the output will thus vary up and down depending upon the relative phase of the two input signals, and will center around 5 volts peak-to-peak. Since the phase comparator will generate a pulse only once for every 500 cycles of the reclocking signal, the average voltage generated is very small. Therefore the signal is peak detected and averaged over a large number of circulations. The smoothed detected signal is applied as bias to the control grid of a reactance tube which in turn varies the frequency of a Hartley oscillator. It was found necessary to use a 0.1 microfarad condenser to couple the 10 megacycles into the reactance tube to eliminate a 60 cps modulation which resulted from the high grid circuit impedances used. The optimum bias for operation of the reactance tube is 2.5 to 3.5 volts. When choosing the proper mode on which to operate, one should be selected where the system will lock in properly on at least one higher and one lower value of voltage. Adjacent modes are approximately 0.7 volts apart. The loop has a control factor of approximately 50.

The oscillator drives the power amplifier at a level of 60 volts peak-to-peak. The power amplifier in turn drives the buffer amplifiers at a level of 3 volts peak-to-peak. The 100 volt peak-to-peak outputs of the buffer amplifiers are used to provide a reclocking pulse to the reclocking gates. In order to increase the impedance in the plate circuits of the buffer amplifiers the cables to the reclocking gates are not terminated with their characteristic impedance. The distributed capacity of the cables form part of the tuned plate loads. The buffer amplifiers are operated Class A to minimize distortion in the reclocking signal. It is important to keep the distortion low at the cable inputs. The reason for this is that the cables will introduce some distortion (as a result of dispersion) because of their improper termination. By using proper cable terminations and locating a buffer amplifier on each DELTIC chassis, the cable distortion could be eliminated.

Transfer Signal Circuits

The schematic diagram, component layout, and a photograph of the transfer signal chassis are shown in Figures 16, 17, and 18, respectively.

The positive sampling pulses are fed to the transfer signal chassis through a convenient length of 950 ohm coaxial delay line at a level of 12 volts peak-to-peak. The pulse shaper and amplifier stretches the pulse to 2.2 microseconds at a level of 100 volts peak-to-peak so as to insure proper action of the counters. Three standard commercial decade counters were used, although two were modified to give the desired performance, which is a square wave output with a repetition rate of one cycle for every five hundred counts. The three counters have a basic count of 1000. By removing the input binary stage of one counter this was reduced to a basic count of 500. However, since the output of a decade counter is not symmetrical with respect to count, but instead is in one state for six counts and the other state for four counts out of each ten, the last decade counter was modified by moving the input binary to the output of the unit to give a count of 500 which is symmetrical with respect to count. An output is obtained from each plate of the binary stage to furnish signals through cathode followers to synchronize the motor on the dielectric recorder. These signals are 180 degrees out of phase and each is 110 volts peak-to-peak at the output of the cathode followers. The enabler is a single shot multivibrator which will remain in its unstable stage after being triggered for a period between 2T and 3T. However, a sufficient amount of the sampling pulse is coupled to the enabler through the counter so that the enabler is returned to

its stable state at the time of the second sampling pulse after being triggered. This gives even greater tolerance to the circuit. The output of the enabler drives the saturable suppressor of the "and" gate to at least 13 volts positive before the occurrence of the next sampling pulse, driving it from its static voltage of -26 volts to the saturated condition. The other input to the "and" gate is the positive sampling pulse. The output of the "and" gate consists of negative pulses of 28 volts peak-to-peak and of 0.1 microsecond duration. A very large plate resistor can be used in the "and" circuit since the pulse load is one of the 2200 ohm resistors in the positive pulse generator which it drives.

The positive pulse generator is a multivibrator which is long term monostable but which can be triggered from its stable state and back again in a short period of time. It is designed to remain in the unstable state up to about 1100 microseconds if not triggered back to the stable state (this is the geometric mean between the length of time it remains in each state in normal operation). This time could increase or decrease by a factor of twenty before trouble would result. The standard form of multivibrator used in counter circuits was found to be unsatisfactory due to the extremely large difference in "on" times between the two tubes, resulting in the "normally off" tube drawing more current than the "normally on" tube. This resulted in a 50% decrease in the output amplitude due to the coupling through the common plate resistor of the two tubes. It was found necessary to eliminate the common resistor. Driving the multivibrator is accomplished through disconnect diodes directly to the plates. In order to obtain stable operation it was necessary to use a sufficiently short time constant in the grid of the "normally on" tube so that the grid returned partially back to zero before the second pulse tripped the multivibrator back to the stable position. To obtain sufficiently flat tops on the positive pulse it was necessary to use a very long time constant on the grid circuit of the "normally off" tube. Pentodes and a two-terminal linear phase shift plate coupling network were used in order to provide adequate rise time. The output drives the power amplifier at a level of 37 volts peak-to-peak. The phase splitter power amplifier output is similar to the one used to supply the sampling signal, except that the coupling capacitors are much larger to prevent sag in the pulse. Outputs are taken from the plate and cathode at a level of 25 volts peak-to-peak to provide the positive and negative transfer input and drop pulses. The negative pulse is also used to drive a 5654 from saturation (grid current limited) to cut-off, thus providing isolated low-impedance positive triggers of 25 volts peak-to-peak for auxiliary equipment such

as the oscilloscope used to display the correlation pattern of the input signals.

Correlator Circuit

The schematic, component layout, and a photograph of the correlator chassis are shown in Figures 19, 20, and 21 respectively. The inputs to the correlator from the DELTICs (at a level of 20 volts peak-to-peak) are first amplified and clipped so that the degradation in the signals resulting from passing down the coaxial delay line cables is largely eliminated. The signals are then added by tying the plates of the clipper amplifiers together. A two-terminal linear phase shift plate-coupling network is used to increase the rise time. Each amplifier contributes a signal of 10 volts peak-to-peak, so the composite signal is 20 volts peak-to-peak at the input to the correlator (a photograph of the composite signal is given in Figure 32). This signal is then biased around +6 volts dc so that the signal varies from -4 volts when both signals are negative to +6 volts when one is positive and the other negative to +16 volts when both are positive. By putting this into the suppressor of a 5725 gate tube with the cathode at ground potential and with a screen potential of 12 volts (thus requiring only a 5 volt swing from cut-off to saturation) a standard pulse of 0.5 volt peak-to-peak is created for both +16 volts and +6 volts on the suppressor, and no pulse is generated for -4 volts on the suppressor. Thus this gate generates a pulse for both positive or for a difference in polarity. If the clipped signal is also introduced into a second gate with 12 volts screen-cathode potential, but whose cathode is at +12 volts a standard pulse will be generated only if both signals are positive. If they are different in polarity, or both negative, no pulse is generated. Since the currents drawn by the various electrodes are quite low the biases are obtained from a heavily by-passed resistive divider network. A moderate amount of integration as well as shielding to prevent feed-through of the reclocking signal is obtained by using coaxial cable to connect the plates of the decision gates to the difference amplifier.

If no signals are present at the inputs to the difference amplifier the two halves draw nominally the same current. If a signal is present at one grid and not at the other the current tends to shift to the tube with no input (negative signals), keeping the total passed by both tubes essentially constant. If signals appear on both grids both tubes reduce current very slightly, since the voltage from cathode to ground is much greater than the amplitude of the signals. The output can be taken from either plate depending on the polarity of the signal desired, and

is 1.6 volts peak-to-peak for signals varying between +100% and -100% correlation. The desired integration time can be conveniently formed by bypassing the plate resistor of the difference amplifier with the proper capacitor. The proper choice will depend on the circulation time (T) of the DELTIC since this is the time required to complete one comparison between the two time series for a given time displacement. Usually it is desirable to make the RC constant somewhat shorter than T for optimum transient response. If a Dielectric Integrator is used the low-pass characteristics of the integrator may be used to provide the integration over T. In such a case, a short integration time should be used in the correlator to preserve the high frequency response of the over-all system. However, since a short integration time on the correlator increases the fluctuations out of the correlator, thus restricting the dynamic range of the Dielectric Integrator, a compromise must be reached which will not affect the over-all frequency response and yet will reduce the fluctuations out of the correlator. In the present system the value chosen was 10 microseconds integration time with T = 50 microseconds. This gives a nominal cut-off frequency for the correlator of 16 kilocycles, whereas the Dielectric Integrator cuts off at about 6 kilocycles. It was necessary to decouple the plate of the difference amplifier from B+ in order to reduce the hum which becomes prominent on the dielectric integrator output with small input signal-to-noise ratios.

The output of the difference amplifier is used to drive a relatively low output impedance variable gain amplifier to obtain maximum dynamic range from the dielectric integrator (since the maximum variation in the signal is about 15 db less for small signal-to-noise ratio than it is for signals varying between +100% and -100% correlation). An output of 30 volts peak-to-peak is obtained at maximum gain for signals varying from +100% to -100% correlation.

Two correlators were built into the present system. With these it is possible to simultaneously perform two autocorrelations, an auto- and a cross-correlation, or cross-correlations delaying each signal. Photographs of the correlator output for a number of different signal conditions are given in Figures 33-40.

Over-all System Notes

1. Power Requirements. The power requirements for the individual components of the system are given in Table I. The -26 volt and 330 volt dc supplies and the 6.3 volt ac need not be regulated. It is desirable to regulate the 220 volt dc, and

necessary to regulate the 150 volt dc supplies. The -9 volts can be obtained from a bias battery. One side of the 6.3 volt ac in all chassis is grounded. Common power supplies can be used for the entire system.

2. Construction. Silver plated copper chassis, point-to-point wiring, and liberal use of rf decoupling circuits in dc and 60 cps ac supply leads are used throughout the system, resulting in reduction or elimination of: grounding problems, interaction between chassis, and dissimilarities between channels. In order to reduce interstage capacitances, and changes in capacitance, a new type of silver plated Lucite slug which was developed by the Missiles Division of NOL was used extensively.

TABLE I

System Component	Current Requirements (milliamperes)					
	330 volt dc	220 volt dc	150 volt dc	-9 volt dc	-26 volt dc	6.3 volt ac
DELTIC	--	---	98	---	4.5	1575
Reclocking & Sampling Signal Chassis	--	60	78	0	1	2525
Reclocking Signal Buffer Amplifier	--	180	42	---	-2	5950
Transfer Signal Chassis	50	2	46	---	6.5	5600
Correlator (single)	--	15	26	---	26	1800

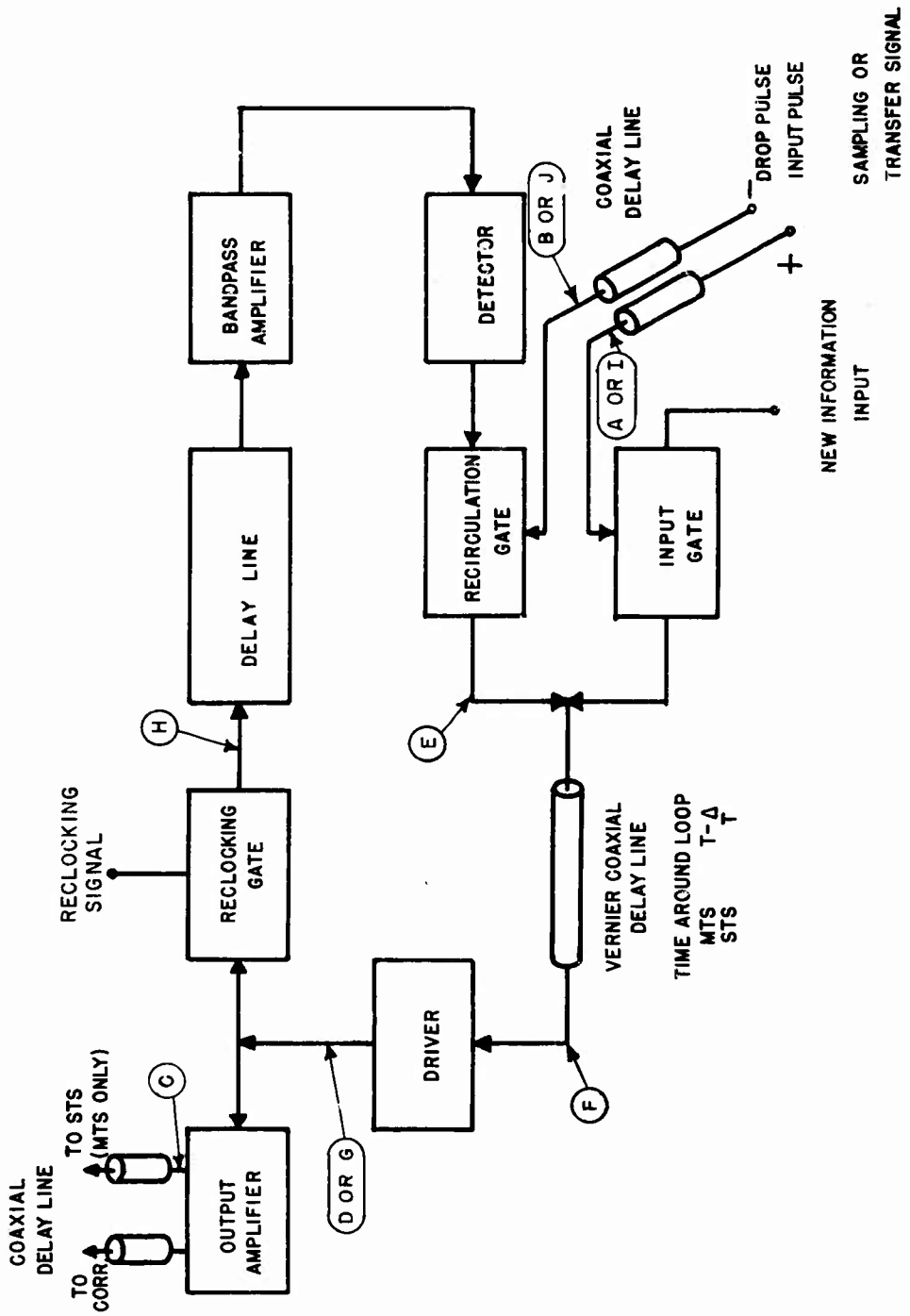


FIG. 1 BLOCK DIAGRAM OF DELTIC CHASSIS (MTS AND STS)

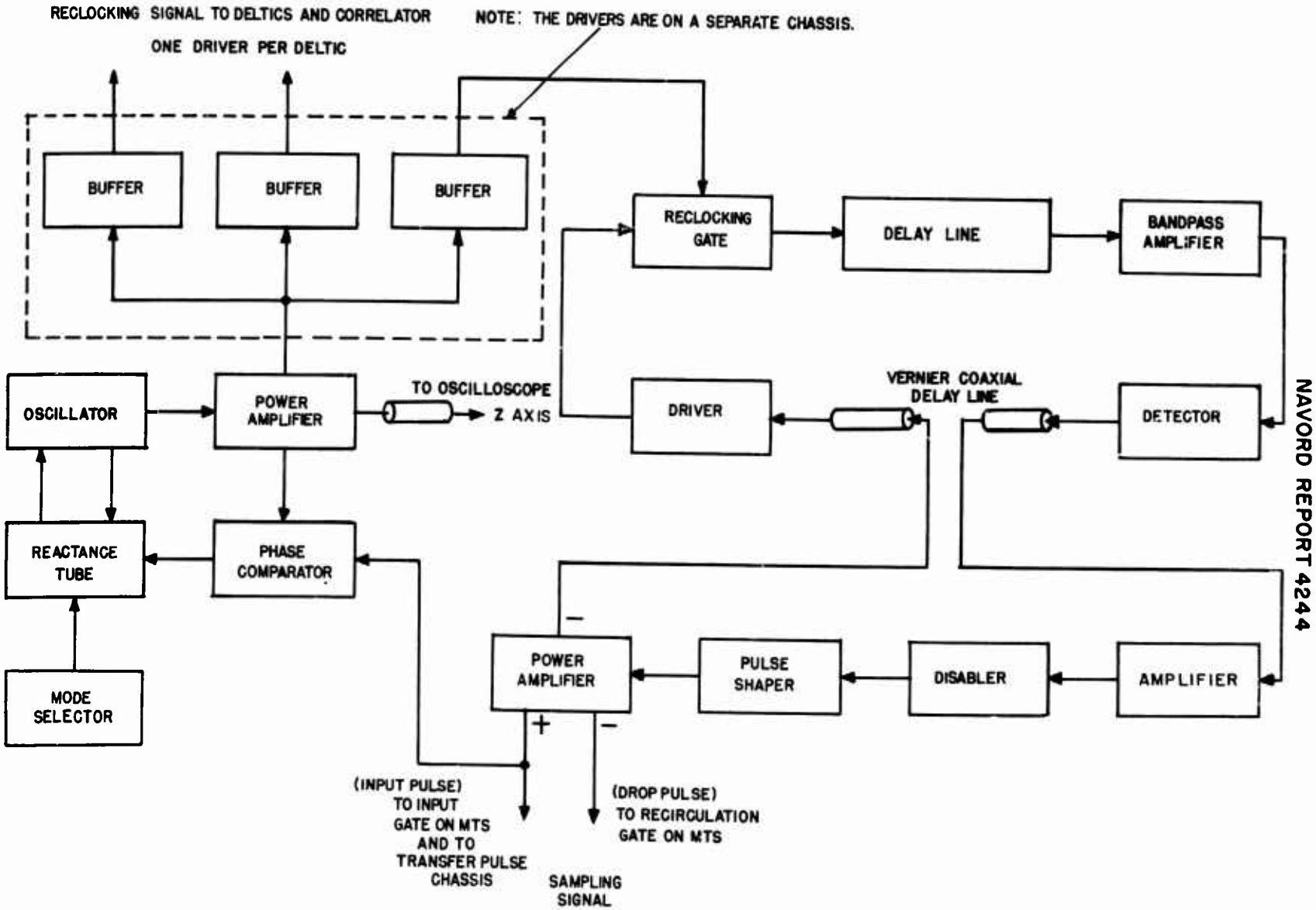


FIG. 2 BLOCK DIAGRAM OF RECLOCKING AND SAMPLING SIGNAL CHASSIS AND DRIVER CHASSIS

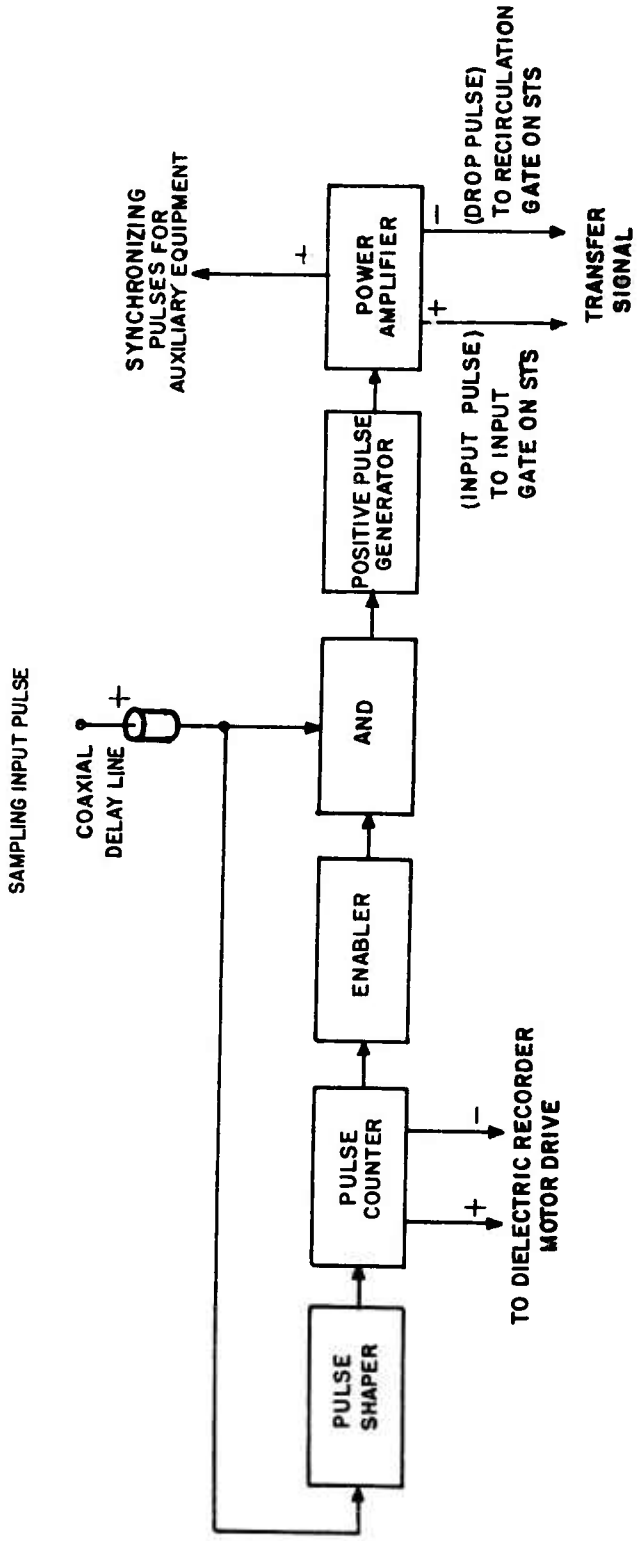


FIG. 3 BLOCK DIAGRAM OF TRANSFER SIGNAL CHASSIS

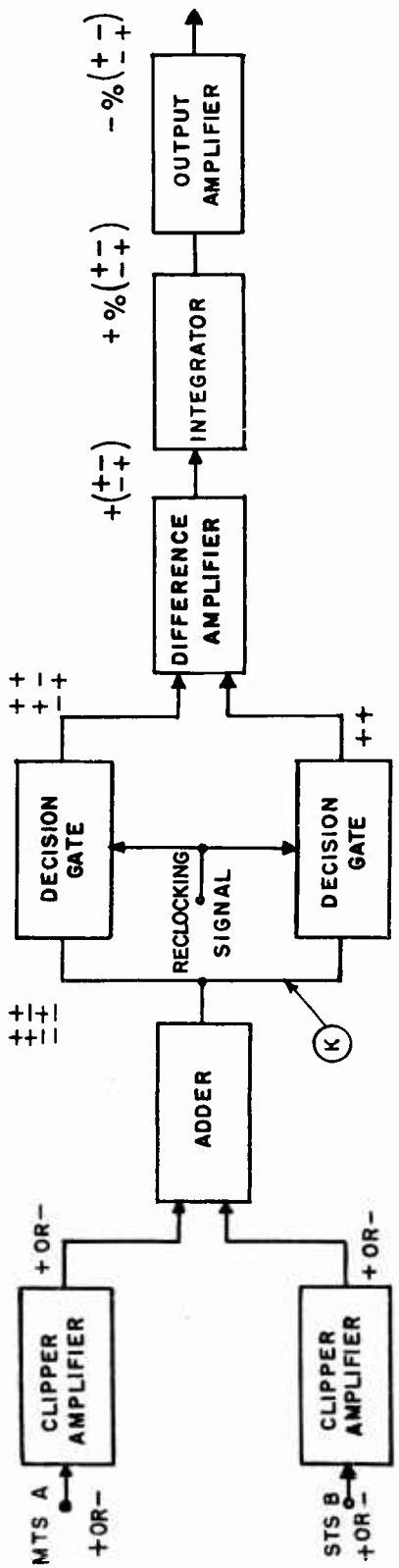


FIG. 4 BLOCK DIAGRAM OF CORRELATOR CHASSIS

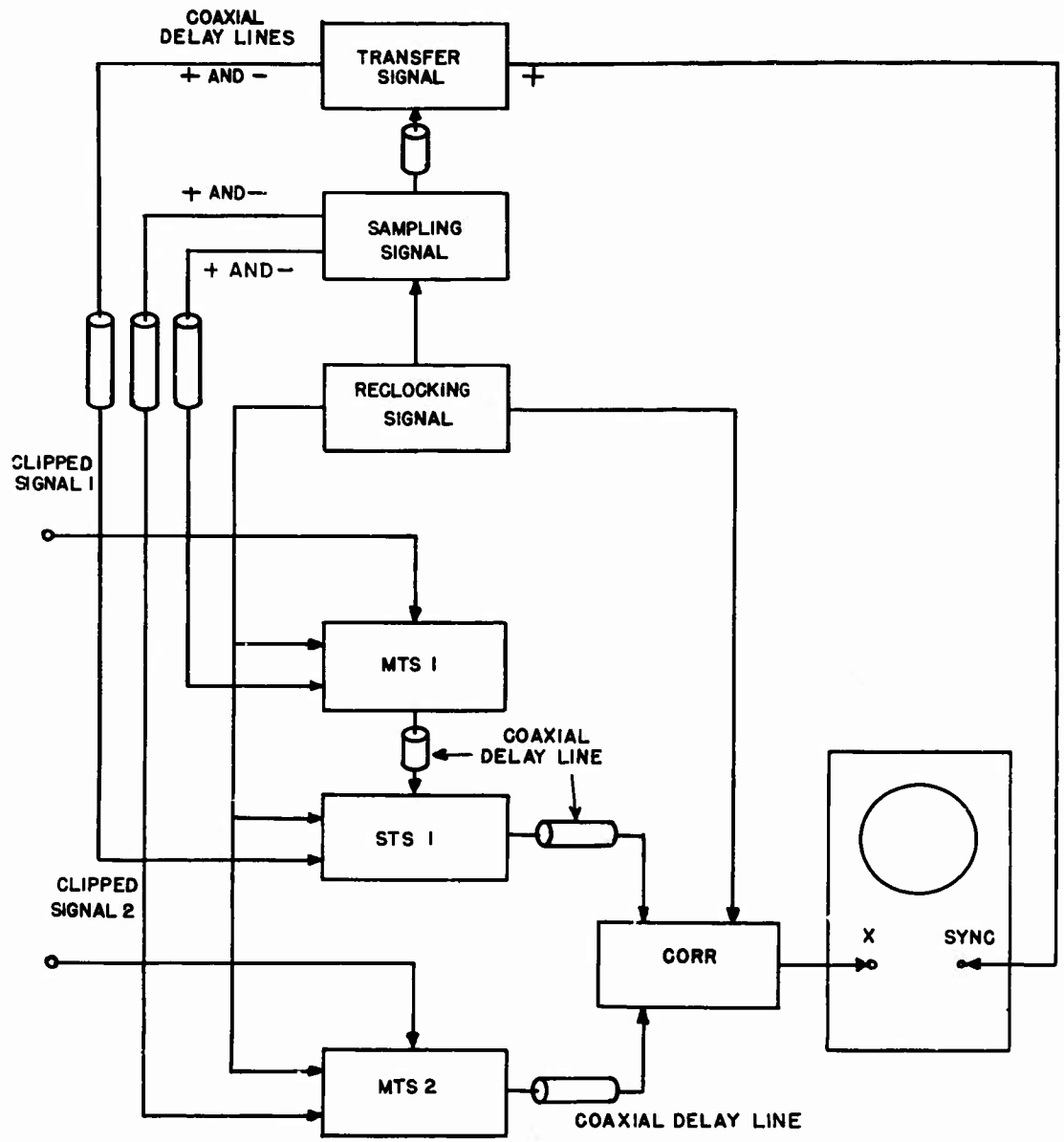


FIG. 5 BLOCK DIAGRAM OF INTERCONNECTING CABLES AND EQUIPMENT REQUIRED FOR CROSS-CORRELOGRAM

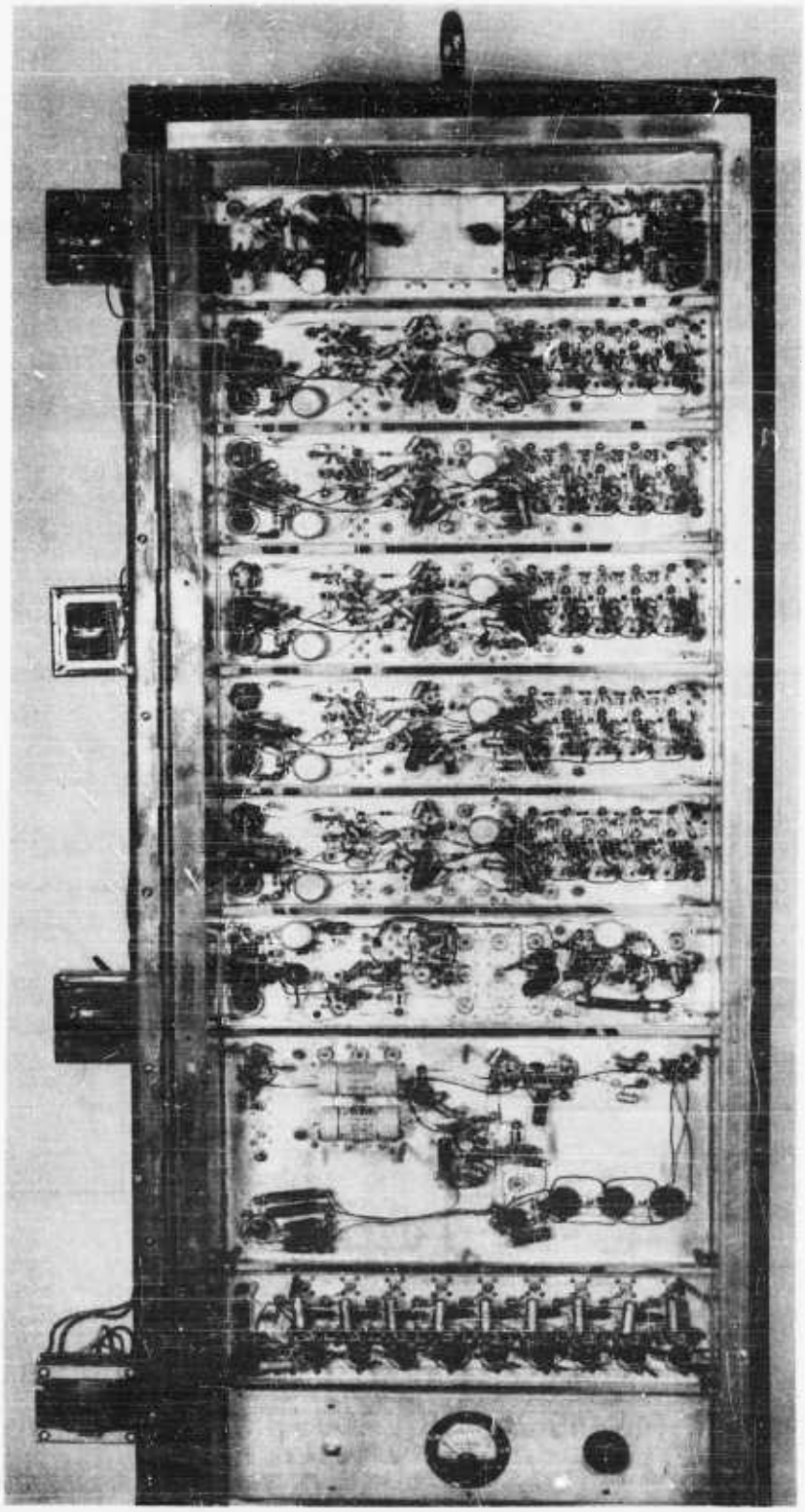


FIG. 6 OVERALL SYSTEM
FRONT VIEW

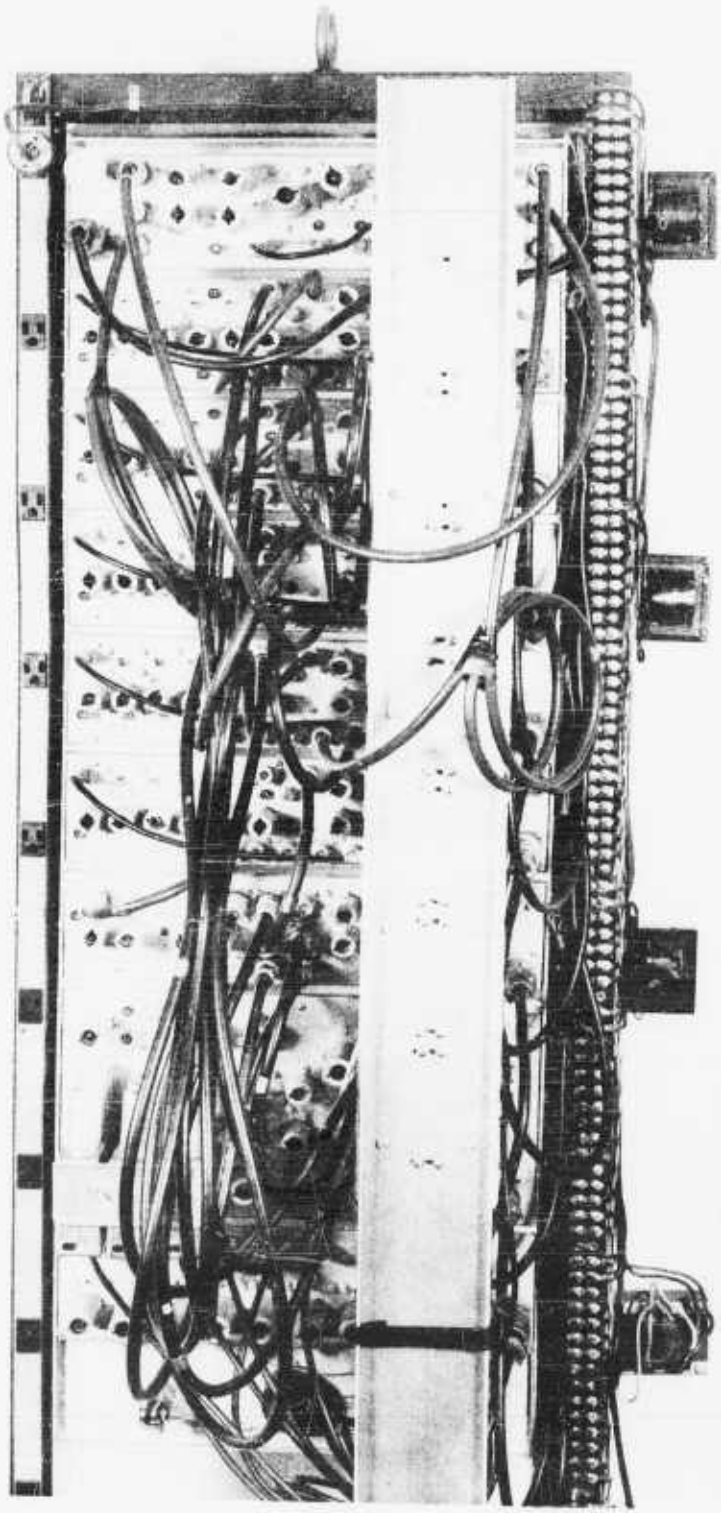
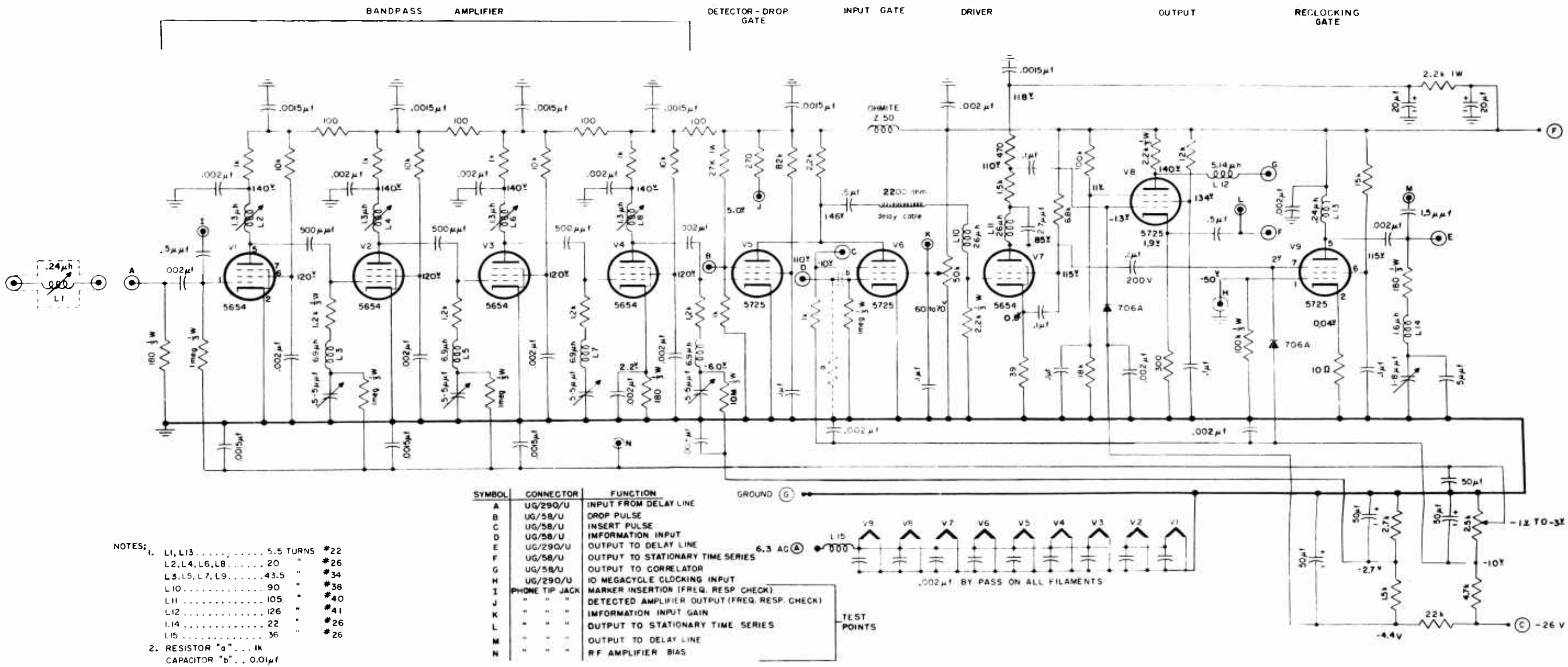


FIG. 7 OVERALL SYSTEM
REAR VIEW



SYMBOL	CONNECTOR	FUNCTION
A	UG/290/U	INPUT FROM DELAY LINE
B	UG/58/U	DROP PULSE
C	UG/58/U	INSERT PULSE
D	UG/58/U	IMFORMATION INPUT
E	UG/290/U	OUTPUT TO DELAY LINE
F	UG/58/U	OUTPUT TO STATIONARY TIME SERIES
G	UG/58/U	OUTPUT TO CORRELATOR
H	UG/290/U	IO MEGACYCLE CLOCKING INPUT
I	PHONE TIP JACK	MARKER INSERTION (FREQ. RESP. CHECK)
J	" " "	DETECTED AMPLIFIER OUTPUT (FREQ. RESP. CHECK)
K	" " "	IMFORMATION INPUT GAIN
L	" " "	OUTPUT TO STATIONARY TIME SERIES
M	" " "	OUTPUT TO DELAY LINE
N	" " "	RF AMPLIFIER BIAS

NOTES;
1. L1, L13 . . . . . 5.5 TURNS #22
   L2, L4, L6, L8 . . . . . 20 " #26
   L3, L5, L7, L9 . . . . . 43.5 " #34
   L10 . . . . . 90 " #38
   L11 . . . . . 105 " #40
   L12 . . . . . 126 " #41
   L14 . . . . . 22 " #26
   L15 . . . . . 36 " #26
2. RESISTOR "a" . . . 1k
   CAPACITOR "b" . . 0.01µf
3. "a" AND "b" USED ON STATIONARY TIME SERIES CHASSIS ONLY.

FIG.8 DELTIC SCHEMATIC

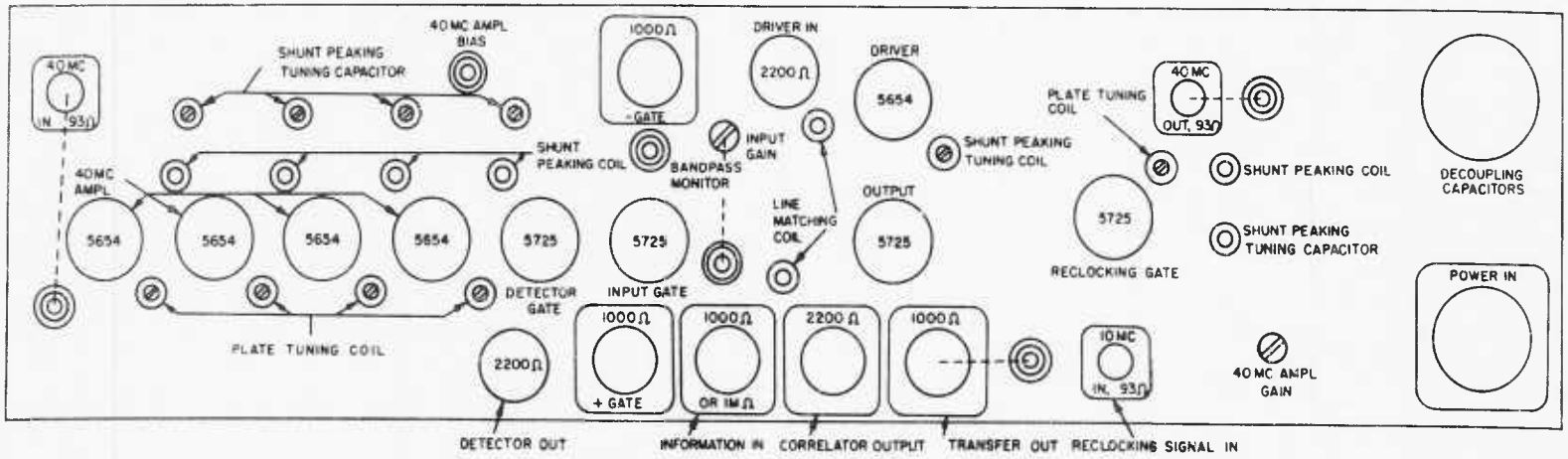


FIG. 9 DELTIC COMPONENT LAYOUT

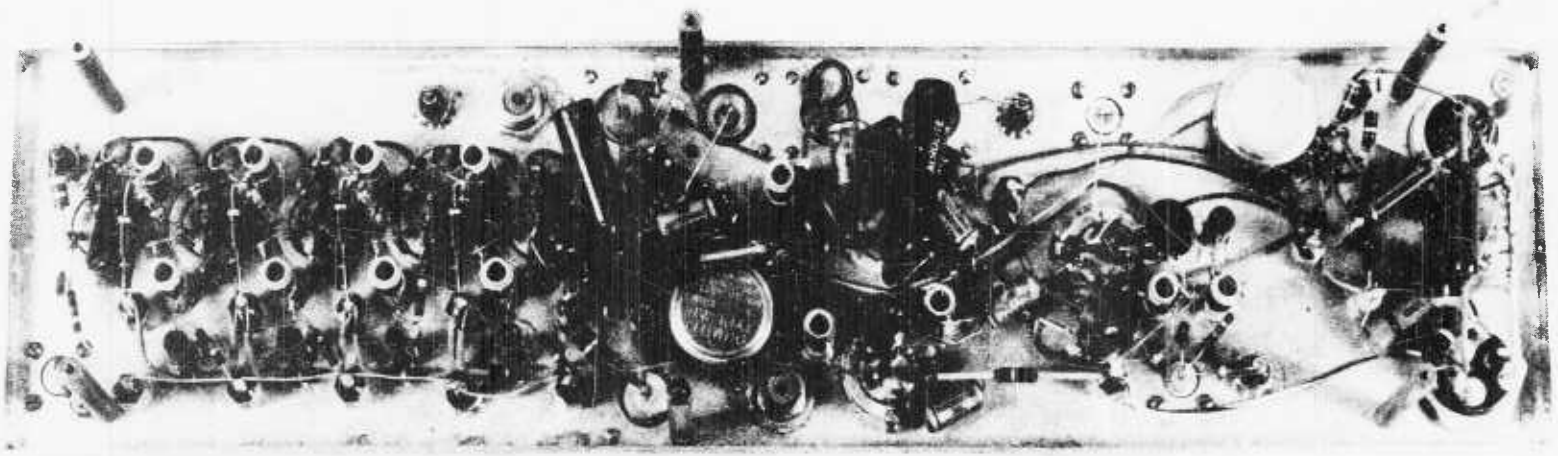


FIG. 10 DELTIC CHASSIS

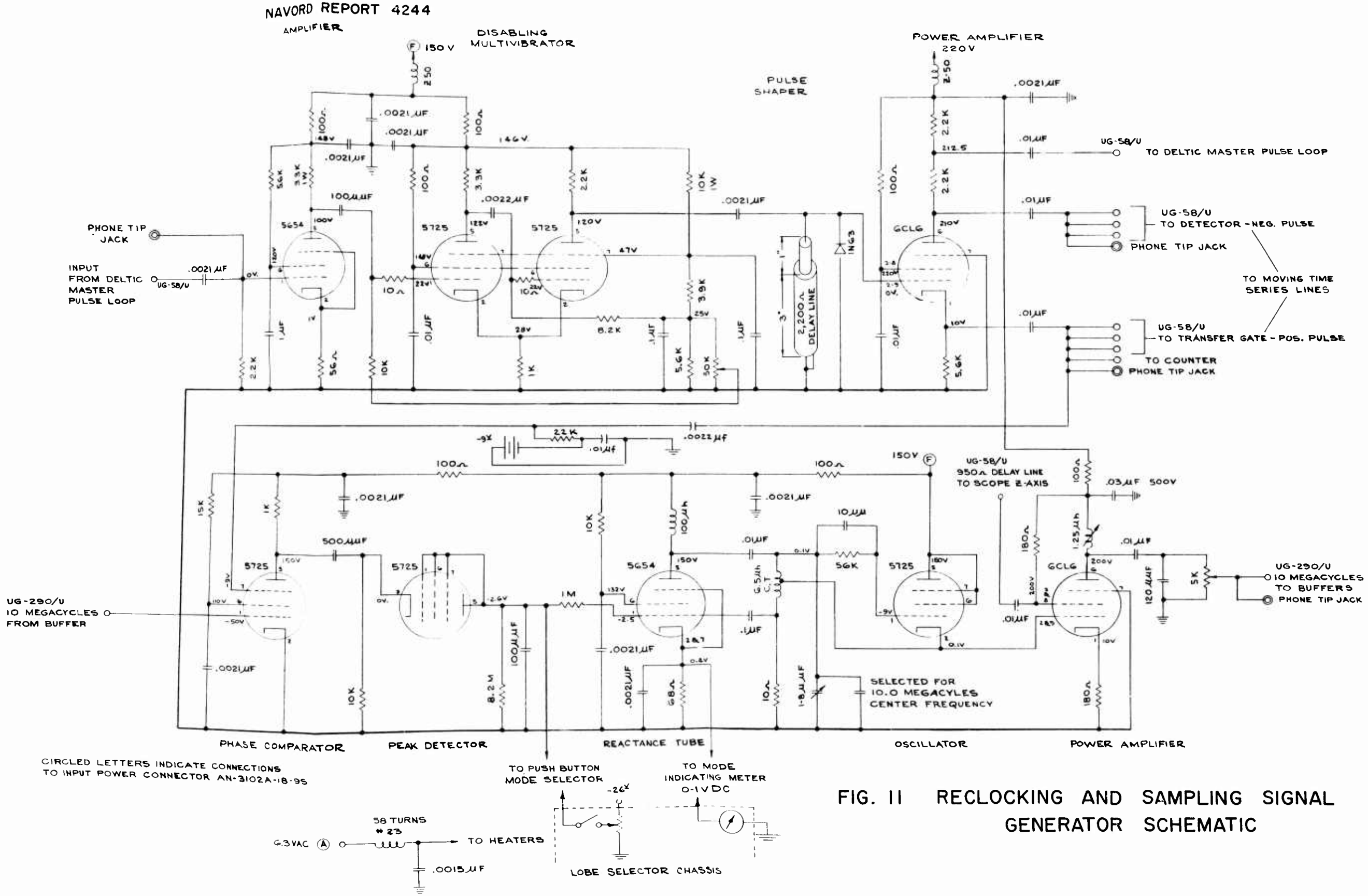


FIG. 11 RECLOCKING AND SAMPLING SIGNAL GENERATOR SCHEMATIC

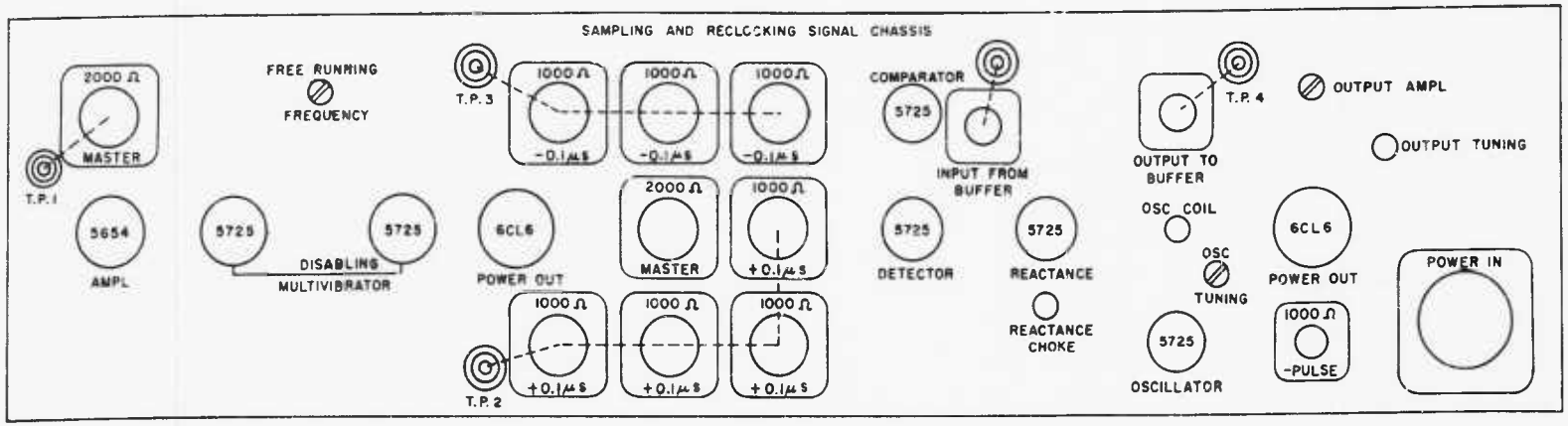


FIG. 12 RECLOCKING AND SAMPLING SIGNAL CHASSIS COMPONENT LAYOUT

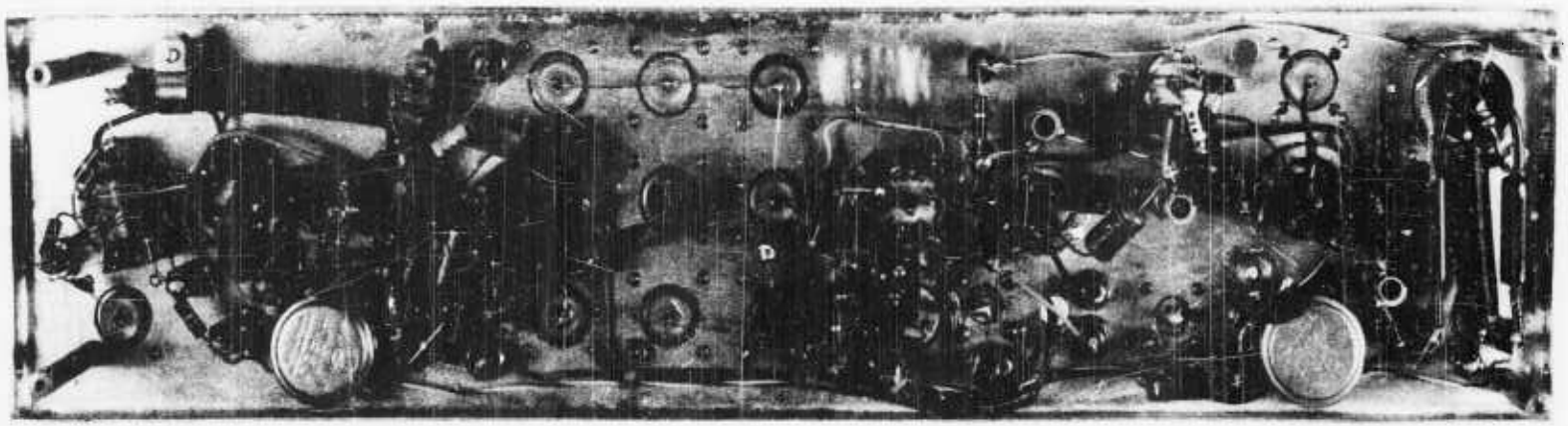


FIG. 13 RECLOCKING AND SAMPLING SIGNAL CHASSIS

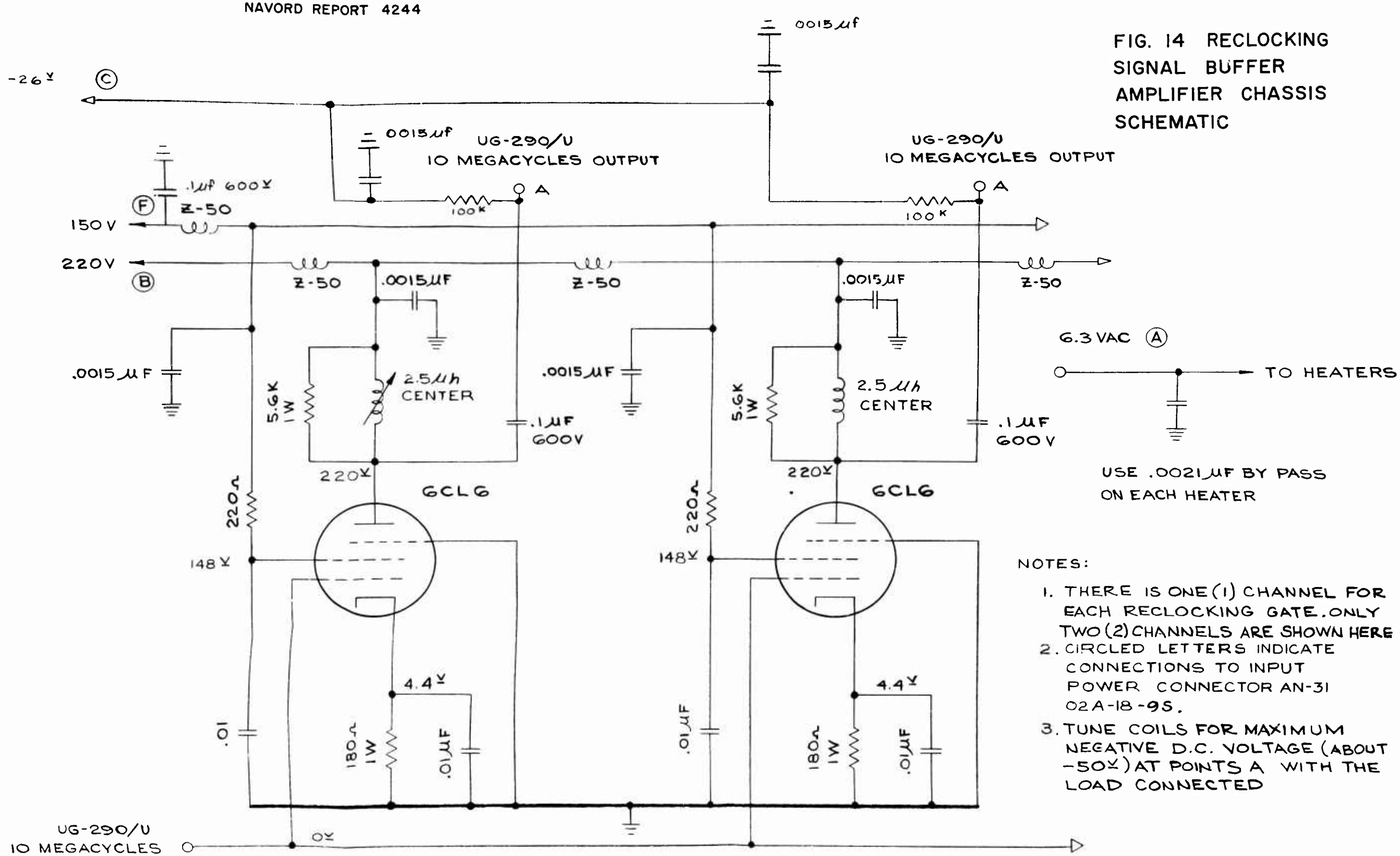


FIG. 14 RECLOCKING SIGNAL BUFFER AMPLIFIER CHASSIS SCHEMATIC

USE .0021μF BY PASS ON EACH HEATER

NOTES:

1. THERE IS ONE (1) CHANNEL FOR EACH RECLOCKING GATE. ONLY TWO (2) CHANNELS ARE SHOWN HERE
2. CIRCLED LETTERS INDICATE CONNECTIONS TO INPUT POWER CONNECTOR AN-3102A-18-9S.
3. TUNE COILS FOR MAXIMUM NEGATIVE D.C. VOLTAGE (ABOUT -50V) AT POINTS A WITH THE LOAD CONNECTED

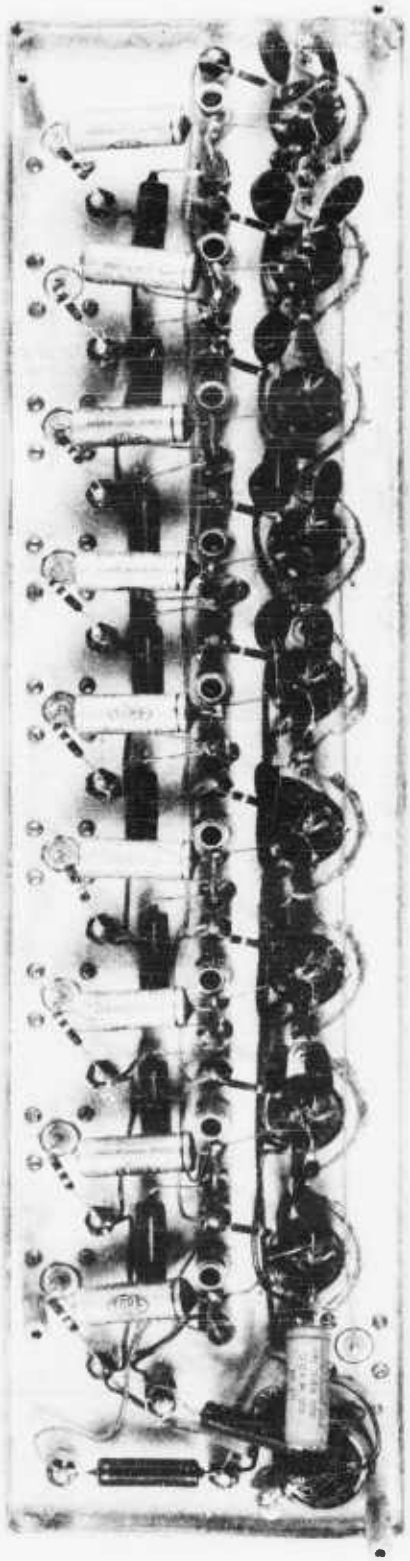


FIG. 15 RECLOCKING SIGNAL BUFFER AMPLIFIER CHASSIS

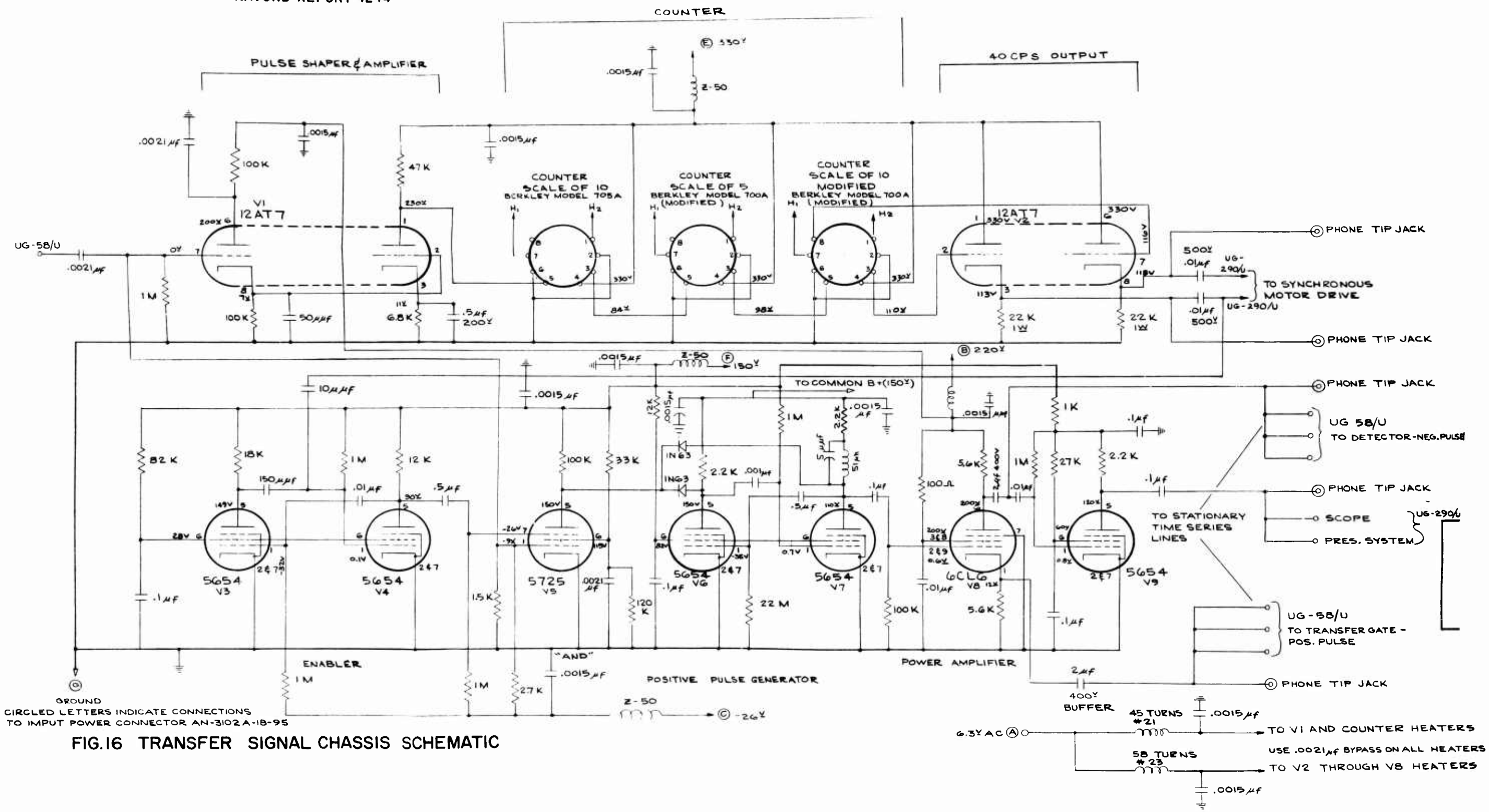


FIG.16 TRANSFER SIGNAL CHASSIS SCHEMATIC

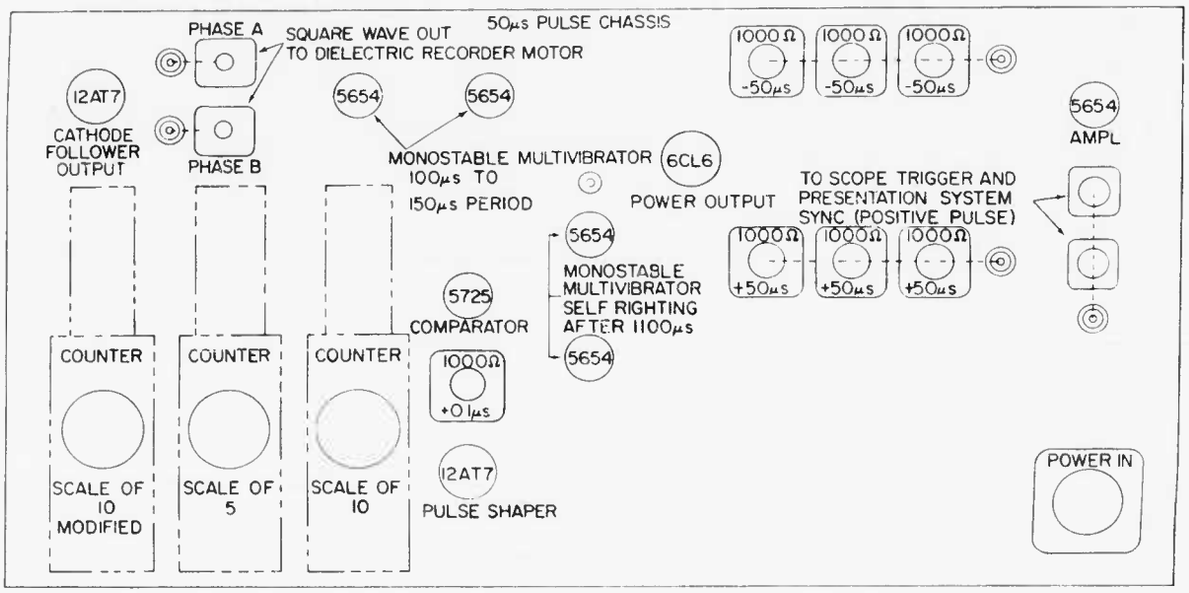


FIG. 17 TRANSFER SIGNAL CHASSIS COMPONENT LAYOUT

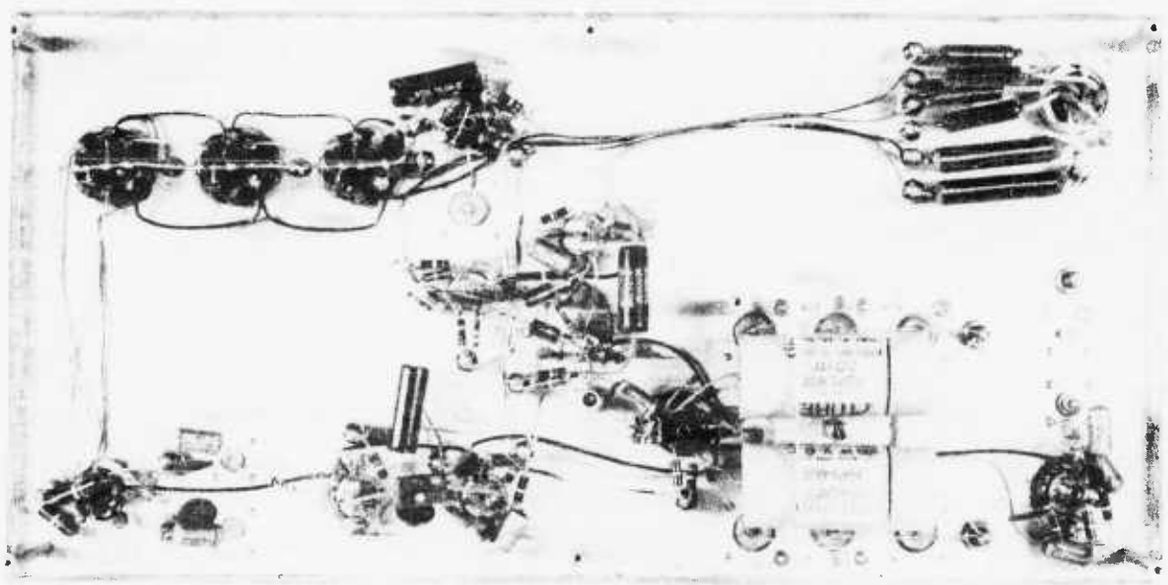
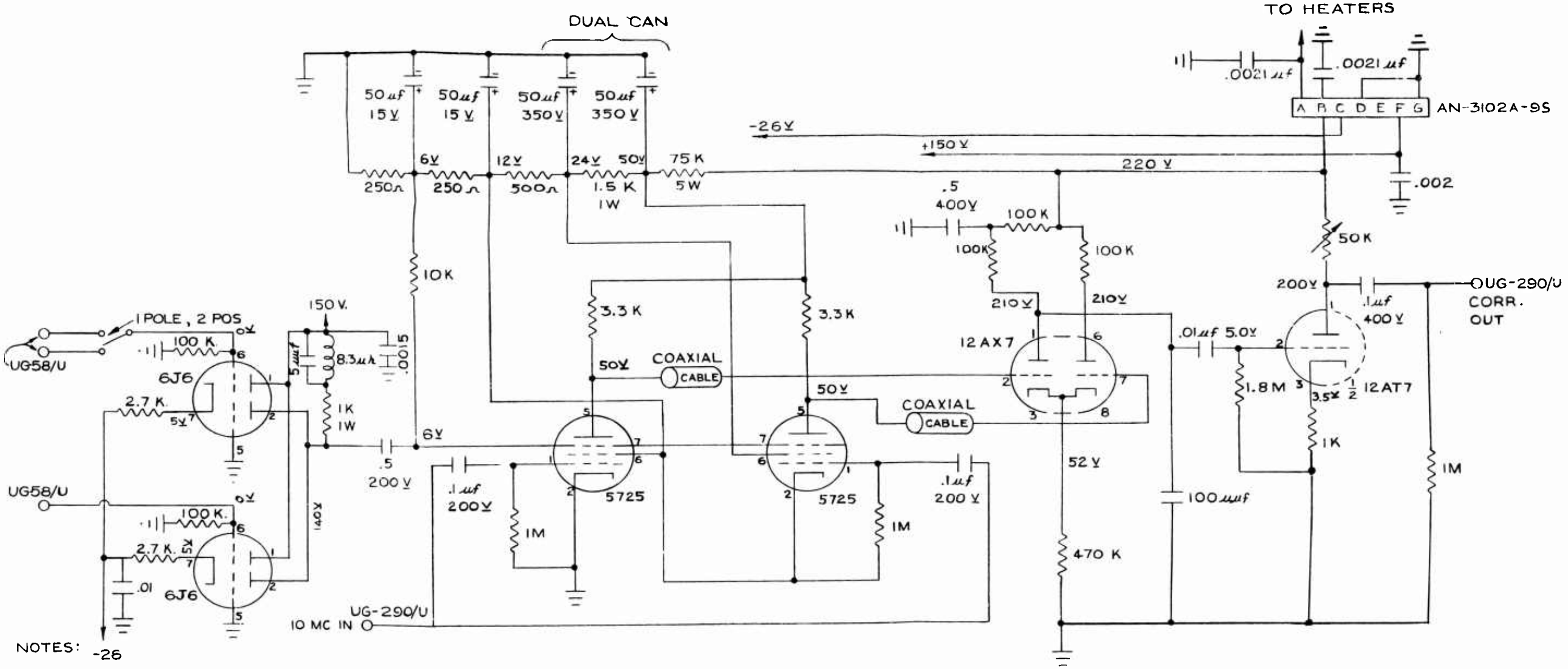


FIG. 18 TRANSFER SIGNAL CHASSIS



NOTES:

1. THIS IS ONE CHANNEL OF TWO CHANNEL SYSTEM.
2. BUILD OTHER CHANNEL AS SHOWN, EXCEPT:
   A. USE SAME VOLTAGE DIVIDER FOR BOTH CHANNELS.
   B. PHASE INVERTER TUBE USES SAME ENVELOPE FOR BOTH OUTPUTS.
   C. POWER PLUG IS COMMON
3. ONE SIDE OF HEATERS IS GROUNDED.
4. BY PASS ALL DC LEADS WITH .0021 μf AT SOCKET OR CLOSEST TIE POINT TO SOCKET.

FIG. 19 CORRELATOR SCHEMATIC

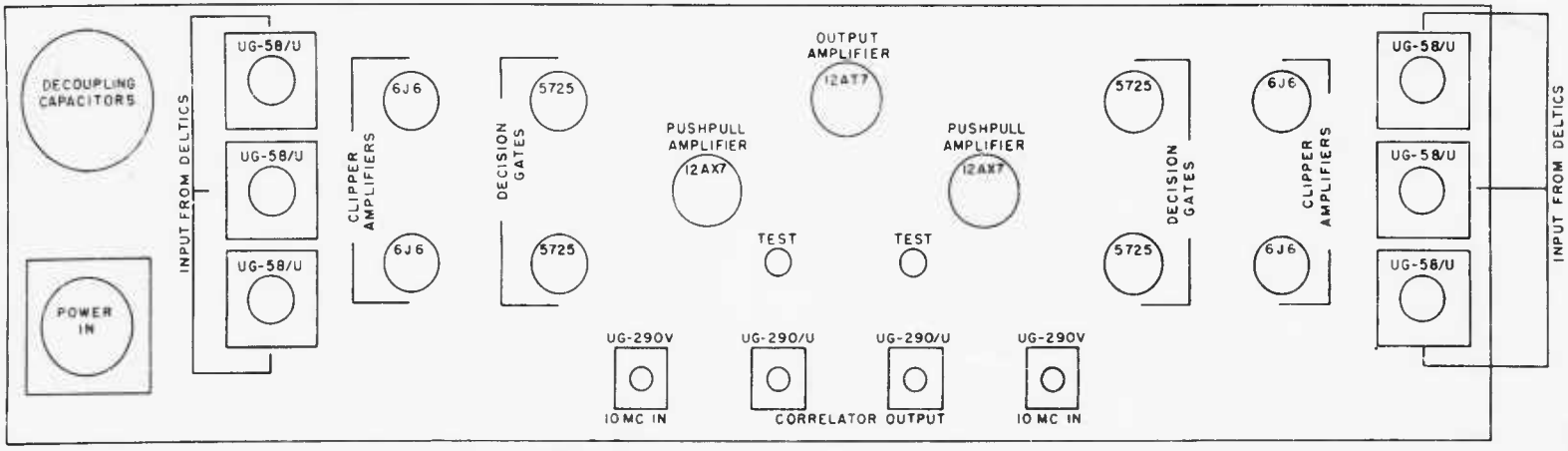


FIG. 20 CORRELATOR COMPONENT LAYOUT

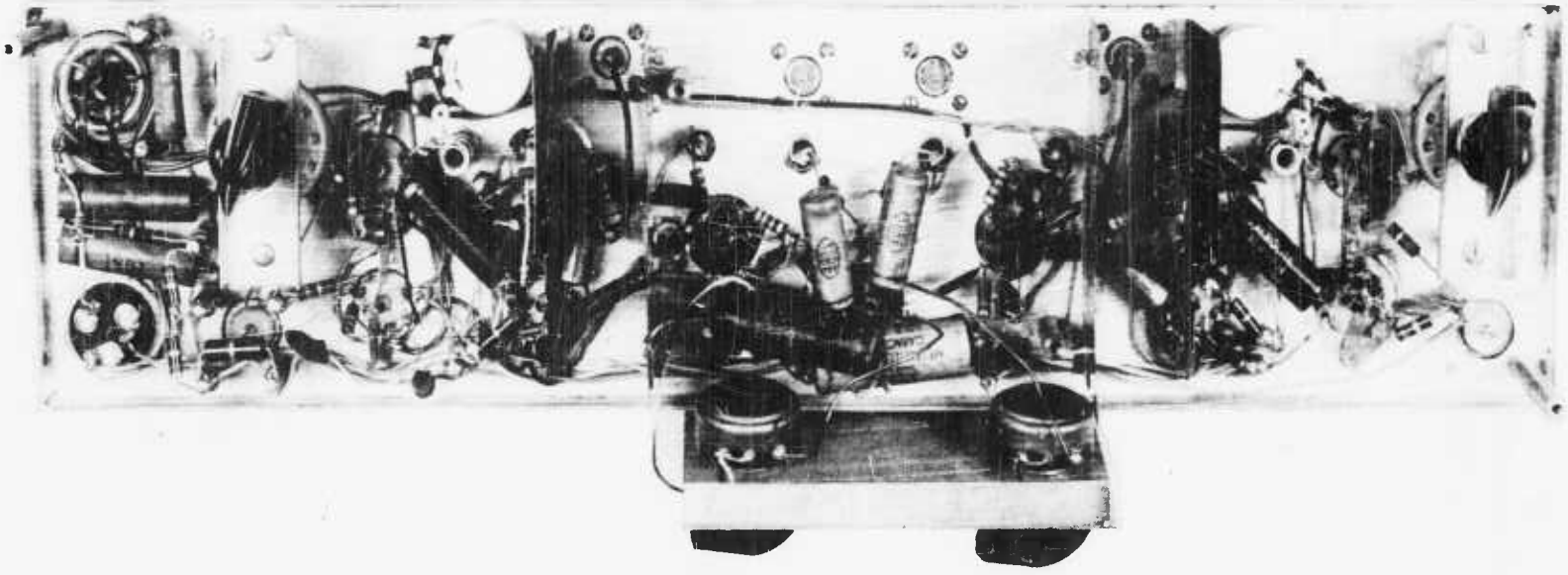
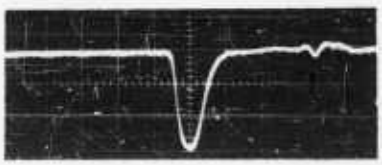


FIG. 21 CORRELATOR CHASSIS

SWEEP SPEED 0.1 μS/MAJOR DIV.
GAIN 5 VOLTS/MAJOR DIV.
CENTERLINE 0 VOLTS DC

Ⓐ FIG. 1

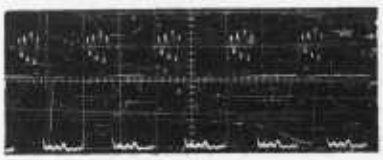
FIG.22 DELTIC MTS SAMPLING INPUT GATE INPUT



SWEEP SPEED 0.1 μS/MAJOR DIV.
GAIN 5 VOLTS/MAJOR DIV.
CENTERLINE 0 VOLTS DC

Ⓑ FIG. 1

FIG.23 DELTIC MTS SAMPLING DROP GATE INPUT

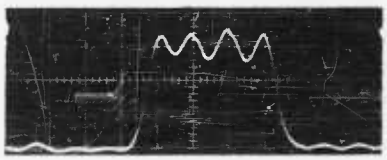


A.

SWEEP SPEED 0.5 μS/MAJOR DIV.
GAIN 1 VOLT/MAJOR DIV.

Ⓒ FIG. 1

TRIGGERED EVERY 25 MILLISECONDS. TRACE WOULD RESEMBLE FIG. 25 IF TRIGGERED EVERY 50 MICROSECONDS

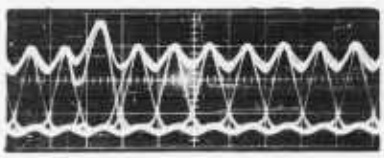


B.

SWEEP SPEED 0.1 μS/MAJOR DIV.
GAIN 1 VOLT/MAJOR DIV.

Ⓒ FIG. 1

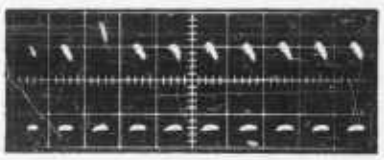
FIG.24 DELTIC MTS OUTPUT STAGE OUTPUT TO STS



A.

SWEEP SPEED 0.1 μS/MAJOR DIV.
GAIN MEANINGLESS
TRIGGER EVERY 50 μS
NOTE CRISS-CROSS PATTERN

Ⓓ FIG. 1

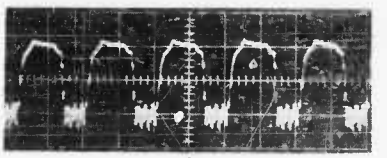


B.

SWEEP SPEED 0.1 μS/MAJOR DIV.
GAIN MEANINGLESS
SCOPE INTENSITY REDUCED SO THAT RECLOCKING SIGNAL BRIGHTENING IS SEEN.

Ⓓ FIG. 1

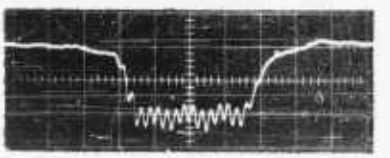
FIG.25 DELTIC MTS RECLOCKING GATE INPUT



A

SWEEP SPEED 0.5 μS/MAJOR DIV.
GAIN 2 VOLTS/MAJOR DIV.

Ⓔ FIG. 1

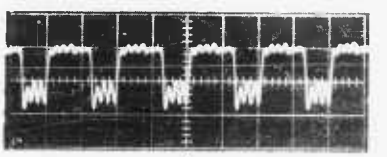


B

SWEEP SPEED 0.1 μS/MAJOR DIV.
GAIN 2 VOLTS/MAJOR DIV.

Ⓔ FIG. 1

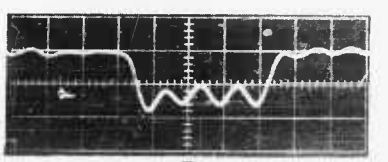
FIG. 26 DELTIC STS DETECTOR OUTPUT



A

SWEEP SPEED 0.5 μS/MAJOR DIV.
GAIN 2 VOLTS/MAJOR DIV.

Ⓕ FIG. 1

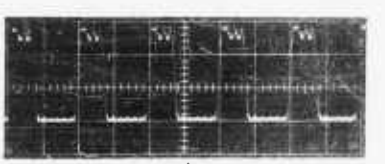


B

SWEEP SPEED 0.1 μS/MAJOR DIV.
GAIN 2 VOLTS/MAJOR DIV.

Ⓕ FIG. 1

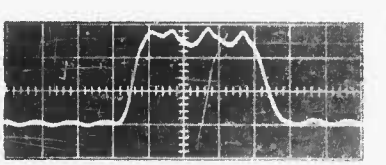
FIG. 27 DELTIC STS DRIVER INPUT



A

SWEEP SPEED 0.5 μS/MAJOR DIV.
GAIN 10 VOLTS/MAJOR DIV.
CENTERLINE 0 VOLTS DC

Ⓖ FIG. 1



B

SWEEP SPEED 0.1 μS/MAJOR DIV.
GAIN 10 VOLTS/MAJOR DIV.
CENTERLINE 0 VOLTS DC

Ⓖ FIG. 1

FIG. 28 DELTIC STS RECLOCKING GATE INPUT

A

SWEEP SPEED 0.5 μS/MAJOR DIV.
GAIN 0.5 VOLTS/MAJOR DIV.

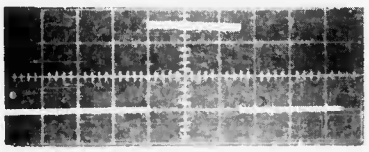
Ⓗ FIG. 1

B

SWEEP SPEED 0.1 μS/MAJOR DIV.
GAIN 0.5 VOLTS/MAJOR DIV.

Ⓗ FIG. 1

FIG 29 DELTIC STS RECLOCKING GATE OUTPUT



SWEEP SPEED 20 μS/MAJOR DIV.
GAIN 10 VOLTS/MAJOR DIV.
CENTERLINE 0 VOLTS DC

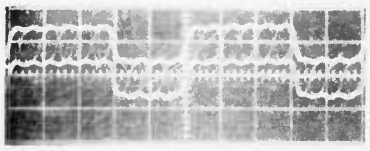
Ⓘ FIG. 1

FIG 30 DELTIC STS TRANSFER INPUT GATE INPUT

SWEEP SPEED 20 μS/MAJOR DIV.
GAIN 10 VOLTS/MAJOR DIV.
CENTERLINE 0 VOLTS DC

Ⓙ FIG. 1

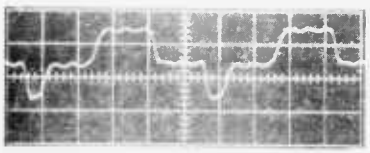
FIG 31 DELTIC STS TRANSFER DROP GATE INPUT



A

SWEEP SPEED 0.2 μS/MAJOR DIV.
GAIN 10 VOLTS/MAJOR DIV.
CENTERLINE 0 VOLTS DC
TRIGGER EVERY 50 μ SECONDS

Ⓚ FIG. 4



B

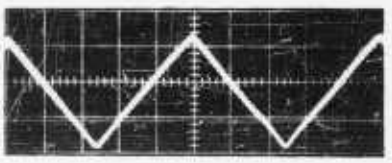
SWEEP SPEED 0.2 μS/MAJOR DIV.
GAIN 10 VOLTS/MAJOR DIV.
CENTERLINE 0 VOLTS DC
TRIGGER EVERY 25 MILLISECONDS

Ⓚ FIG. 4

FIG. 32 CORRELATOR ADDED OUTPUT OF CLIPPER AMPLIFIERS

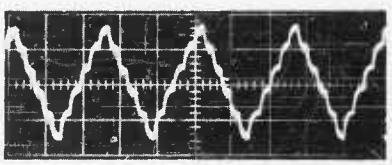
SWEEP SPEED — 5 MILLISECONDS/MAJOR DIV.
GAIN — 10 VOLTS/MAJOR DIV.

FIG. 33 CORRELATOR OUTPUT-INPUT 40 CPS S/N = ∞



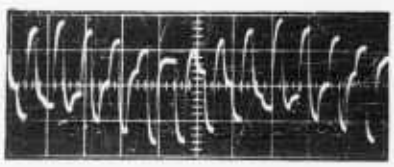
SWEEP SPEED — 0.5 MILLISECONDS/MAJOR DIV.
GAIN — 10 VOLTS/MAJOR DIV.

FIG. 34 CORRELATOR OUTPUT-INPUT 400 CPS S/N= ∞



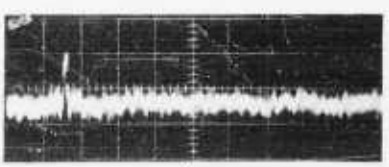
SWEEP SPEED — 0.2 MILLISECONDS/MAJOR DIV.
GAIN — 10 VOLTS/MAJOR DIV.

FIG. 35 CORRELATOR OUTPUT-INPUT 2000 CPS S/N= ∞



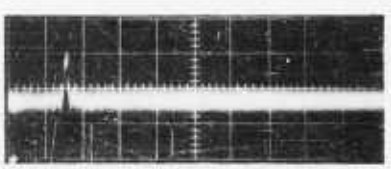
SWEEP SPEED — 0.2 MILLISECONDS/MAJOR DIV.
GAIN — 10 VOLTS/MAJOR DIV.

FIG. 36 CORRELATOR OUTPUT-INPUT 6700 CPS S/N= ∞



A

SWEEP SPEED — 1.0 MILLISECONDS/MAJOR DIV.
GAIN — 10 VOLTS/MAJOR DIV.
EXPOSURE — 1/25 SECOND



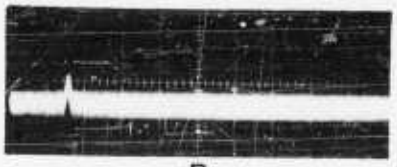
B

SWEEP SPEED — 1.0 MILLISECONDS/MAJOR DIV.
GAIN — 10 VOLTS/MAJOR DIV.
EXPOSURE — 20 SECONDS

FIG. 37 CORRELATOR OUTPUT-INPUT NOISE 200 - 5000 CPS S/N = ∞

A

SWEEP SPEED	1.0 MILLISECONDS/MAJOR DIV.
GAIN	10 VOLTS/MAJOR DIV.
EXPOSURE	1/25 SECOND



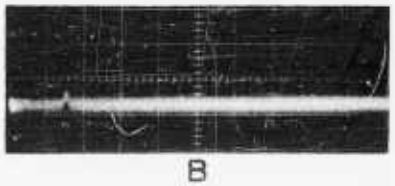
B

SWEEP SPEED	1.0 MILLISECONDS/MAJOR DIV.
GAIN	10 VOLTS/MAJOR DIV.
EXPOSURE	20 SECONDS

FIG. 38 CORRELATOR OUTPUT-INPUT NOISE 200-5000 CPS S/N = 0 DB

A

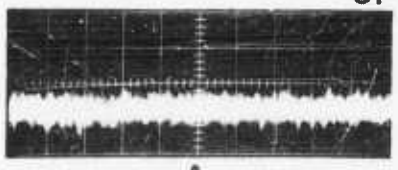
SWEEP SPEED	1.0 MILLISECONDS/MAJOR DIV.
GAIN	10 VOLTS/MAJOR DIV.
EXPOSURE	1/25 SECOND



B

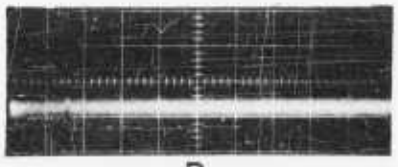
SWEEP SPEED	1.0 MILLISECONDS/MAJOR DIV.
GAIN	10 VOLTS/MAJOR DIV.
EXPOSURE	20 SECONDS

FIG. 39 CORRELATOR OUTPUT-INPUT NOISE 200-5000 CPS S/N = -5 DB



A

SWEEP SPEED	1.0 MILLISECONDS/MAJOR DIV.
GAIN	10 VOLTS/MAJOR DIV.
EXPOSURE	1/25 SECOND



B

SWEEP SPEED	1.0 MILLISECONDS/MAJOR DIV.
GAIN	10 VOLTS/MAJOR DIV.
EXPOSURE	20 SECONDS

FIG. 40 CORRELATOR OUTPUT-INPUT NOISE 200-5000 CPS S/N = -10 DB

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